Publication guidelines for semiconductor plasma-etch technology

Harry J. Levinson
JM[3] Editor-in-Chief

Plasma-etch technology is an integral and indispensable part of patterning technology that has enabled continuous scaling in the semiconductor industry for several decades. The criticality of etch processes became even more apparent during the era when multiple patterning was used to advance scaling, while more recently it has been learned that a proper assessment of stochastic defects must include collection of data post-etch. Going forward, it is expected that etch technology will continue to be a critical part of nano-patterning, particularly for three-dimensional (3D) logic and memory devices, such as 3D FinFET, Gate All-Around (GAA) FET, 3D NAND flash memory as well as 3D dynamic random access memory (DRAM).

With this in mind, publication guidelines are provided in this editorial for papers where plasma-etch technology is central to the presented thesis. These guidelines aim to achieve a balance between the inclusion of key data in published papers and the protection of crucial proprietary information. For the parameters listed below, inclusion for most should be considered as a requirement when relevant to the paper. The etch process parameters can be considered as a possible exception, since it is understood that these are often quite sensitive for the authors' organizations and sometimes cannot be published.

In some papers, post-etch data are included as important elements, but the etch processes themselves are not primary subjects of the papers. For such papers, a lower level of detail than what is specified below is adequate. However, the significance of data will be appreciated better by inclusion of detail, and authors of papers for which etch is not the primary subject should consider this when deciding what information to include.

Plasma-Etch Technology Guidelines

- Type of etching: isotropic or anisotropic
- Type of etch
    - By state: wet or dry
    - By purpose: patterning, resist strip, cleaning, etc.
    - By etching methods
        - Ion milling, plasma processing, remote or chemical etch
    - By mechanism: oxidation, reduction
    - By gas chemistry: O_2, halogen, N_2, NH_3, etc.
    - By etching process
        - Continuous wave
        - Power and/or gas pulsing
        - Cyclic
            - Atomic layer etch (ALE)
            - Quasi-atomic layer etch (QALE)

© 2021 Society of Photo-Optical Instrumentation Engineers (SPIE)

  - Method for addressing etch near wafer edge
  - Method to address etch uniformity

- Plasma sources
  - Remote plasma versus direct plasma
  - Inductive coupled plasma
  - Capacitive coupled plasma
  - Other plasma sources

- Mechanism of etch (for papers focused on new etch tools and processes)
  - Plasma physics
  - Plasma and surface interactions
  - Sidewall passivation mechanisms
  - Damage mitigation

- Film stack
  - Integration flow
    - Photoresist type
      - Examples
        - Chemically amplified resist (CAR)
        - Metal-containing resist (MCR)
    - Etch hard mask: material and thickness
    - Material to be etched: material (metal or dielectric) and thickness
    - Etch stop layer
  - Etch selectivity
  - Multi-color etch

- Etch figures of merit
  - Etch selectivity
  - Etch rate
  - Aspect ratio
  - Sidewall angle
  - Footing
  - Recess
  - After etch inspection (AEI) LER/LWR
  - AEI defectivity
  - Etch uniformity (LCDU or within wafer CDU)
    - Loading and micro-loading, i.e., pattern density impact
  - Profile symmetry across full wafer
  - Throughput

- Etch process parameters (optional)
  - Gas and gas composition (flow rates)
  - Carrier gas and flow rate
  - Pressure

  - RF power
  - Bias
  - Wafer electrode area
  - Temperature
  - Time
  - Endpoint
    - Include metrology, timed etch, etc.
  - Over etch
- Metrology: refer to previously published guidelines

Acknowledgments

We would like to thank the following people for their contributions in the generation of these guidelines: Dr. Qinghuang Lin (primary author), Lam Research Corp.; Dr. Timothy A. Brunner, ASML; Dr. Martin Burkhardt, IBM; Dr. Mircea Dusa, imec; Dr. Frederic Lazzarino, imec; and Dr. Keren Kanarik, Lam Research Corp.