Tough road ahead for device overlay and edge placement error

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ABSTRACT

During the last several years we have seen an impressive drive in the industry to continue to innovate in order to keep up with the challenging requirements of overlay in multi-patterning processes. A major part of these efforts is spent in opening up of the flexibility in control knobs on process tools (mostly lithography and etch) enabling the high order actuation capability. In order to feed this high order actuation, it has also become important to address the need of input data accuracy, driving up the demand for improved metrology accuracy and sampling. Adding to the complexity, it has also become important to address edge placement error (EPE). EPE is basically the pattern fidelity of a device structure created by a multi-patterning process, defined as the relative displacement of the edges of two features from their intended target position. Here local CD error is an important parameter in addition to overlay. EPE requirements of a "single digit nanometer number" is now a harsh reality in 5nm nodes and below.

In this technical presentation we will review the above developments and remaining gaps in technology (litho and dimensional metrology applications), as well as design and integration. Mitigation of such challenges need a large team effort that is industry-wide and not just limited to litho.

Keywords: Overlay, Edge Placement Error, EPE, diffraction, DBO, scatterometer, metrology, accuracy, robustness, device, multi wavelength, color mixing

1. INTRODUCTION

In multi patterning processes, overlay is now entangled with CD including OPC and stochastics[1]. This combined effect is called Edge Placement Error (EPE) and it is the key metrics for patterning budget generation and holistic patterning control. EPE is a serious challenge for continued shrink (scaling) driving down the allowed overlay margin to an unprecedented level. We need to do everything to improve overlay (device overlay) where accurate measurement and control of wafer deformation is extremely important. This requires accuracy in overlay measurement that decouples target asymmetry from wafer deformation (make overlay metrology immune to target asymmetry, so it can measure wafer deformation accurately).

The presence of target asymmetry increases the chance of making an overlay measurement error and variation of asymmetry creates a wafer level (both intra and interfield) as well as a wafer to wafer variation of the error[2]. This significantly weakens the efficiency of a feedback process control loop. The implementation of signal formation physics in the fundamentals of overlay metrology algorithms and hardware have given us a significant boost towards addressing target asymmetry. This has resulted in multi-color overlay metrology techniques[2] that has brought us closer to the truth. These are great achievements for the industry. However there are still gaps. To some extent the measurement photons are blind to the context of the target, it does not know where the real center of gravity of the target is. There is also an ADI to AEI delta due to etch, stress release etc.. Hence it has become important to start measuring device overlay after etch. Keeping in mind the increased need in both accuracy and sampling, a good cost effective hand shake between after develop overlay (on target) and after etch overlay (on device) is needed to close this gap. Both optical and e-beam metrologies need to work together here.

Many of the learnings in target asymmetry mitigation found in overlay metrology also applies to scanner alignment and this synergy helps further to boost accuracy and robustness of overlay. This important angle will also be discussed here.

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But even if we address the gaps in overlay and alignment related items above, it is not fully solving the overall need that requires to also address EPE. The challenging patterning requirements of EPE can only be achieved by using a holistic approach that combines wafer metrology overlay / CD (optical and e-beam), computational optimization of mask (including OPC), the high order actuation capability of the DUV, EUV scanners as well as co-optimization with other processes (deposition, etch). This means the solution space is not limited to lithography only, we must connect, co-work, co-optimize among various process steps to address the tough overall challenge.

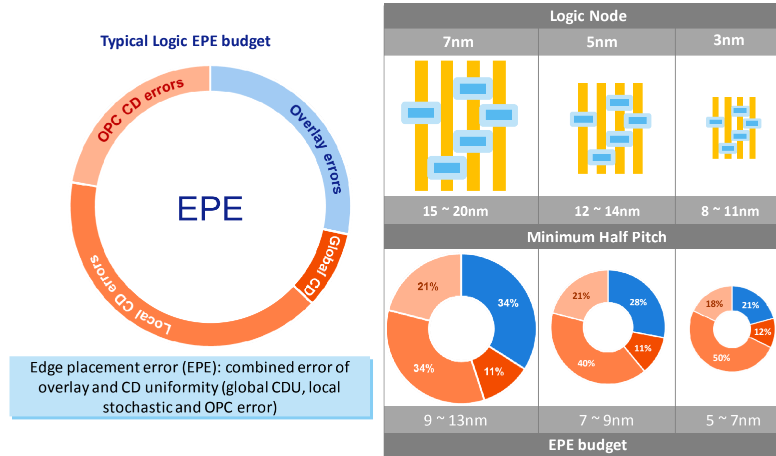

Figure 1. Edge placement error is the main challenge for continued shrink where local stochastic plays a big role

2. HOLISTIC APPROACH TAKEN TOWARDS DEALING WITH THE ISSUE

Three main points to address in device overlay and EPE.

2.1 Address local variation

Maximizing process window with patterning process, Source Mask Optimization (SMO) and OPC address a part of it, but it is important to quantify the remaining stochastic part so it can be compensated by tightening the other budget items.

Much work is already published on how to reduce local variations with co-optimization of patterning processes[9]. This is not discussed in this paper.

SMO data shows a global CDU and local stochastic EPE reduction where 15% local CDU is reduction is possible without compromising other performance metrics.

SMO (global) cost function (CF) evaluates:

$$\mathrm{CF} = \sum_{\mathrm{pw,e}} w_{pw,e}(EPE^n + w\,PPE^n)$$

- Edge Placement Error (EPE) and,
- Pattern Placement error (PPE)

SMO superposes stochastics EPE band

- Local CD variation

$$\mathrm{sEPE} = \frac{a}{blur_ILS^b}$$

a and *b* calibrated to full stochastic resist model or wafer data

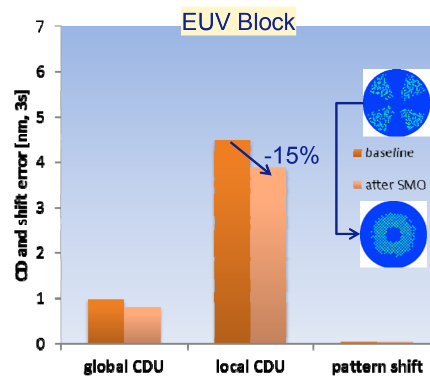

Figure 2. SMO reducing local stochastic

Improving OPC accuracy with more pattern coverage by the use of fast eBeam measurement system, accurate contour metrology and deep learning models helped to improve the systematic part of this local variation.

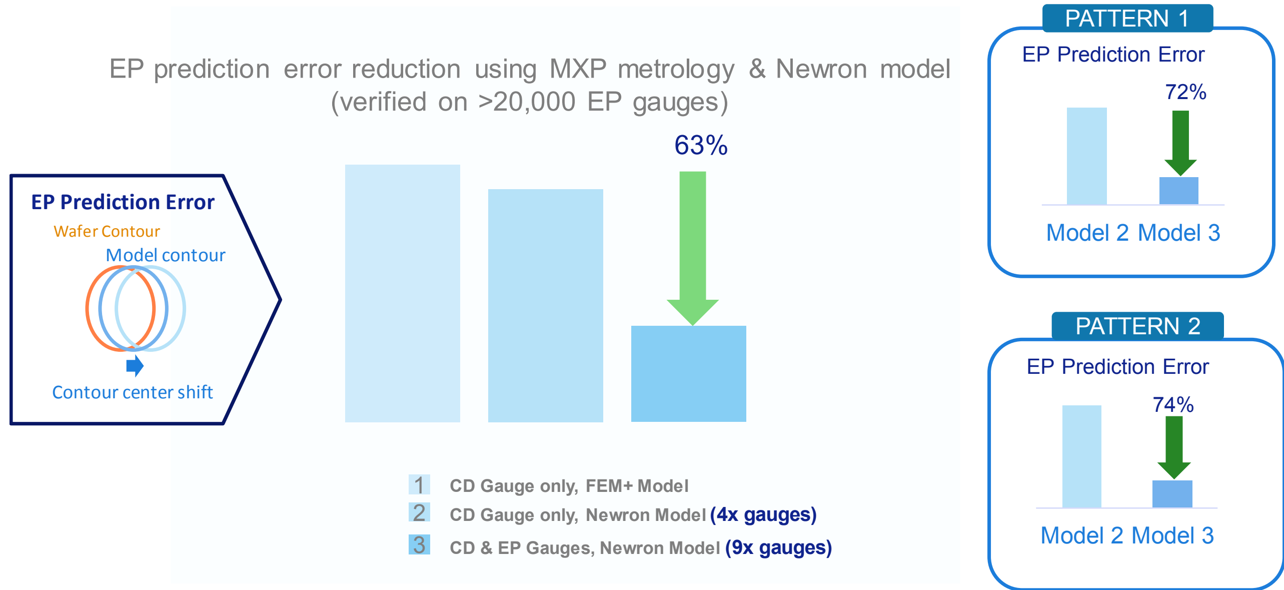

Figure 3. Edge Placement (EP) Prediction Error Reduction by improving OPC error

2.2 Accurate measurement and control of wafer deformation

Decouple target asymmetry from wafer deformation (make overlay metrology immune of target asymmetry, so it can measure wafer deformation accurately) is the main task here.

Overlay is calculated using the measured asymmetry signal of an overlay target. Ideally, the signal used to compute overlay only consists of the asymmetry signals produced by the overlay between top and bottom gratings. In reality, process-induced asymmetry[2] (e.g., grating asymmetry and grating imbalance) also contributes to the above measured asymmetry signal. This is one of the sources of an overlay measurement error and it is recipe dependent (wavelength and polarization). Moreover, when asymmetry is present, a symmetric stack variation (e.g., thickness, n & k etc.) can also influence the magnitude of the overlay error.

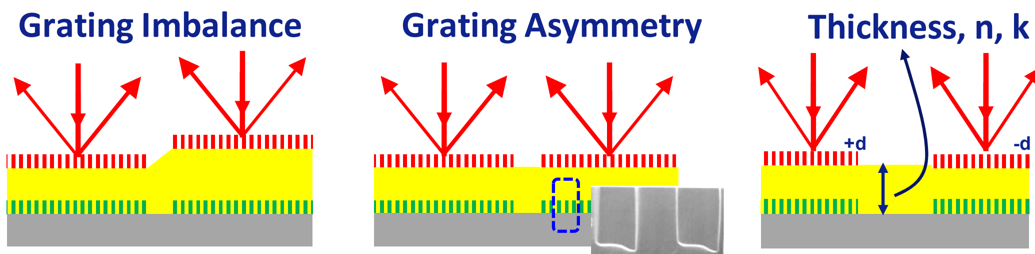

Figure 4. Key challenges in overlay metrology from process induced variations

When no asymmetry is present, overlay measurement is a relatively simple task. Any measurement wavelength or polarizations will be accurate. However, when asymmetry is present, measured overlay is affected and it shows a swing phenomenon (these are shown using a simulation in figure 5).

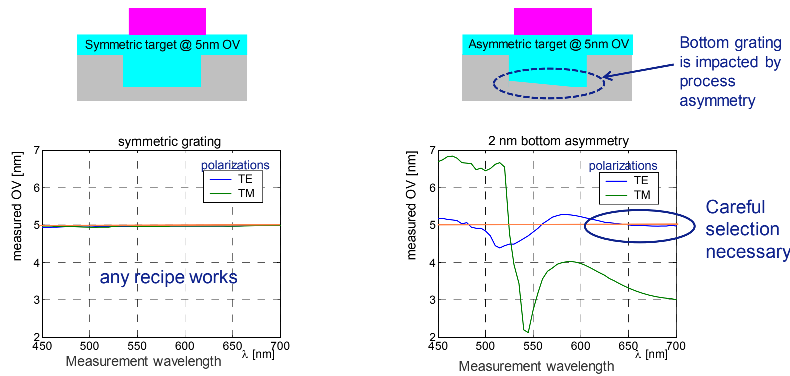

Figure 5. A simulation (using signal formation physics) to show the impact of grating asymmetry on overlay

When asymmetry is present[1,8], a careful selection of recipe is necessary to minimize the error in overlay and such selection procedures were discussed in previous publications[2,3]. For the majority of the production stacks at current production nodes, these procedures are adequate (e.g., selection of a single wavelength / polarization condition that operates near the peak of the signal swing curve). But there are still some cases where these single wavelength approach cannot provide the necessary accuracy. Such cases continue to appear in advanced nodes where process variations continue to dominate while the requirements tighten towards accuracy and robustness of the measurement from wafer to wafer and lot to lot. A few examples on such robustness issues are: a best single-wavelength recipe cannot cover both the center and the edge of a wafer due to process variation over the wafer; a best single-wavelength condition determined at setup is no longer valid in the subsequent lots etc.

When asymmetry is present, each measurement site may be susceptible to an overlay error which will vary with:

(a) Variation of asymmetry over wafer; (b) Variation of symmetric stack parameters (thin film thickness etc.) over the wafer; (c) Field location specific grating imbalance. Controlling overlay in a fab gets more challenging as all of the above can vary from wafer to wafer and lot to lot.

Goal is to eliminate these errors in overlay measurement.

In order to address the above challenge a multi wavelength approach is taken. This is synonymous to an "YieldStar Self-Reference" (YSSR) creation and was discussed in previous publications[2,4]. Overlay calculated with multi wavelength (instead of a single wavelength) using this method[2] (shown below) inherently corrects for the asymmetry error in overlay.

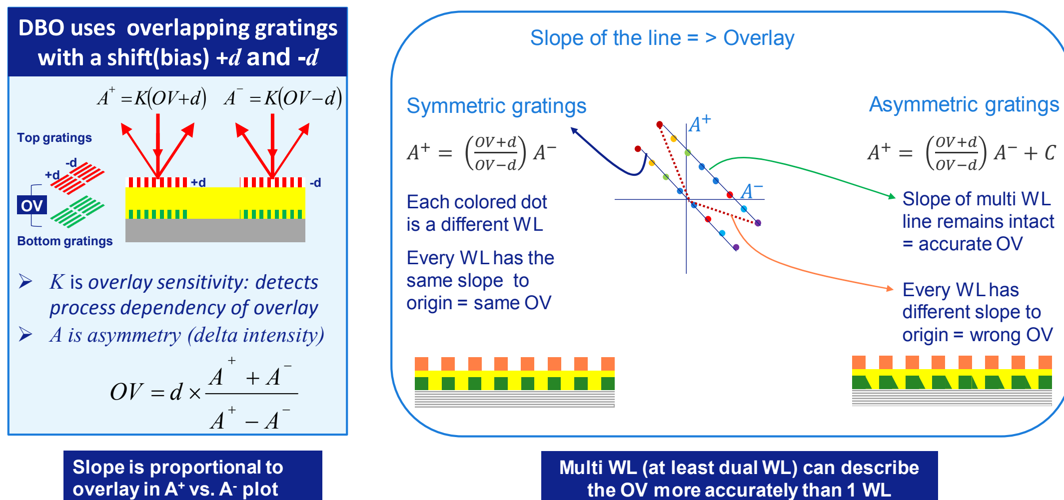

Figure 6. Multi wavelength approach to overlay

But the problem is not fully solved: for a small % of stacks in presence of large asymmetry, a non-linear contribution to overlay exists as shown in figure 7 and this needs to be addressed.

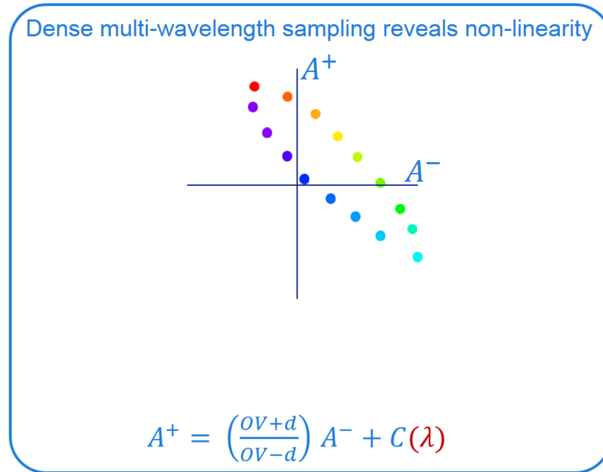

Figure 7. Non-linearity or this ellipse-like phenomenon needs to be addressed

Analysis revealed that this non-linear behavior is caused by a local asymmetry variation within the overlay grating. This shows that we need to not only reduce the impact of asymmetry in global level, but that we should also look for asymmetry variation within a target. We therefore need to have an algorithm that will filter out these asymmetry (non-linear pixels). This requires the measurement to see the full target radiometric image (available via image plane detection[4] with a large metrology spot) in order to avoid areas on the grating that are adversely impacted by processing effect.

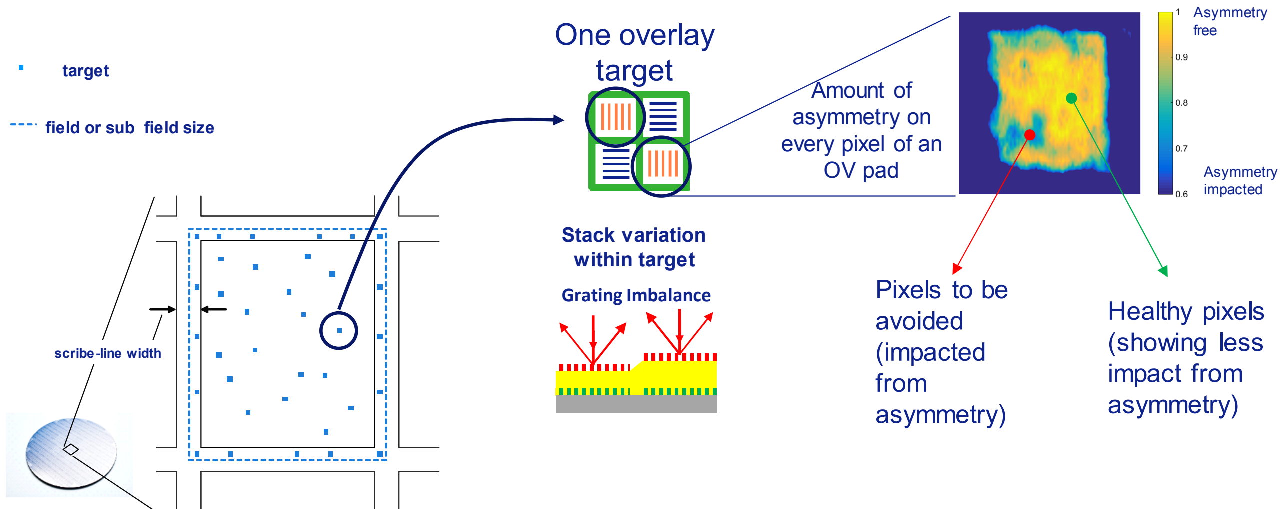

Figure 8. target level asymmetry exists

The overlay roadmap continues to drive the need for higher metro sampling (w/ high order correction) Computational metrology is positioned to mitigate this increase in sampling. Computational Metrology predicts dense overlay maps on all wafers using already available scanner sensor data (level sensor, alignment, stage servo etc.) combined with overlay metrology.

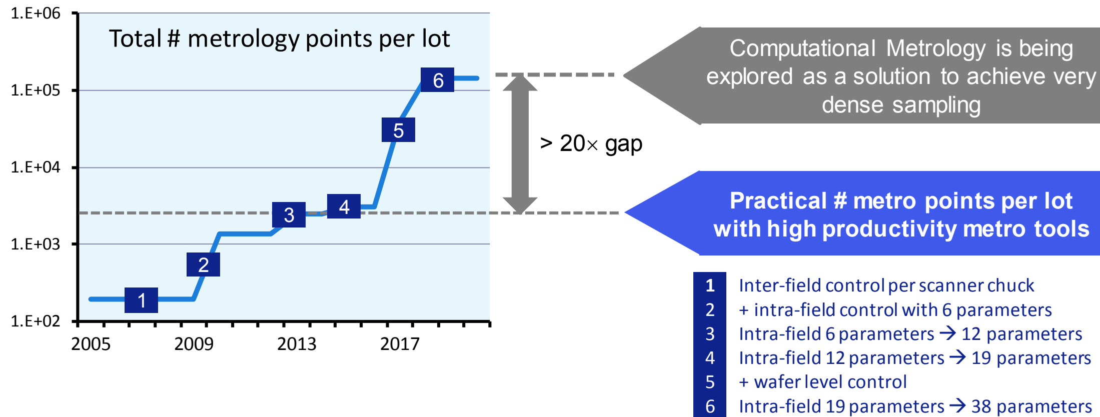

Figure 9. Computational metrology to combine scanner metrology and overlay metrology to generate dense metrology

2.3 Best overlay control obtained by overlay metrology feedback coupled with scanner metrology feedforward (Alignment, Leveling)

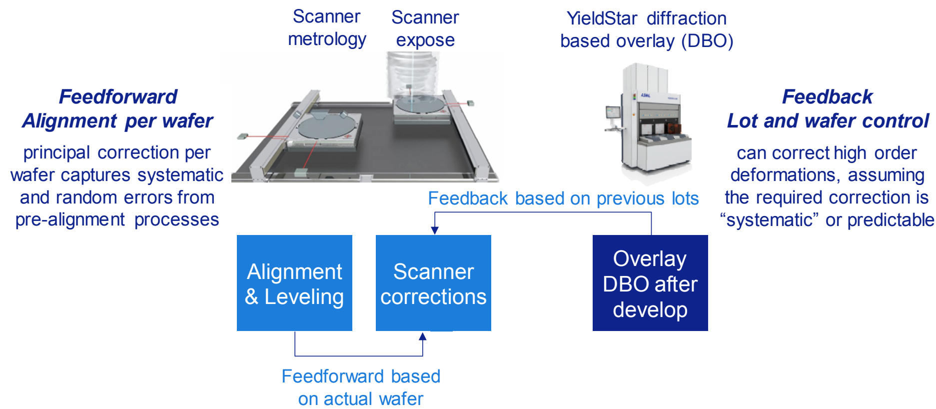

Figure 10. Feed-back and Feed-forward control

Combining Leveling and Alignment results in a dense overlay grid that can be used for better OV control.

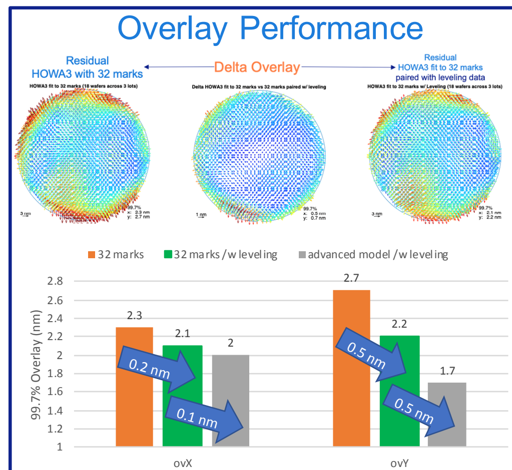

Figure 11. Combining Leveling and Alignment results in a dense overlay grid that can be used for better OV control

2.4 Path towards addressing device overlay

Even though computational metrology can predict extreme dense overlay map, it is still the overlay after develop (ADI OV) and still needs calibration / validation using real measured data on device after etch (AEI OV). This drives towards after etch metrology where measurements can be done directly on device. Measurement directly on device removes the limitation on the number of dedicated targets that needs to be placed on a product mask. Now the question is how much and how often do we need to measure AEI overlay: can we live with the speed of HVSEM? Do we need the high speed of optical metrology (in case of run-time correction) ?

Data shows that significant delta between after develop overlay (measured on OV targets) vs. after etch overlay (measured on device) exists.

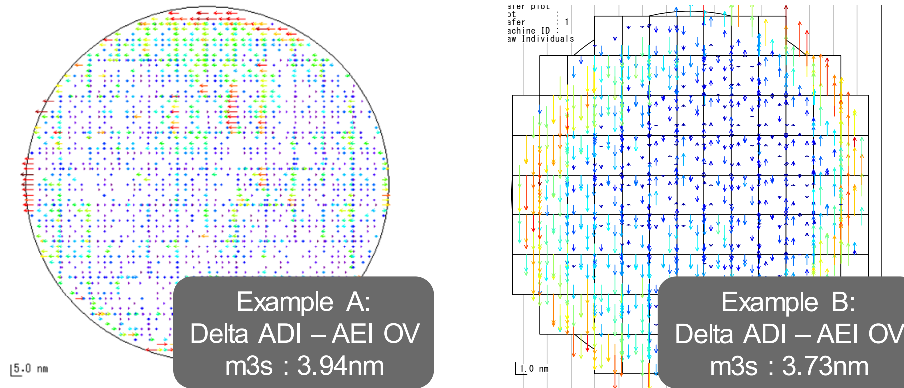

Figure 12. Delta fingerprint after-etch to after-develop

A dynamic control using after etch overlay (measured on device) showing benefit over static control; this means:
1. ADI vs. AEI overlay delta is varying run-time
2. Need a high speed after etch overlay metrology for this feedback control (e.g., optical metrology as used below)

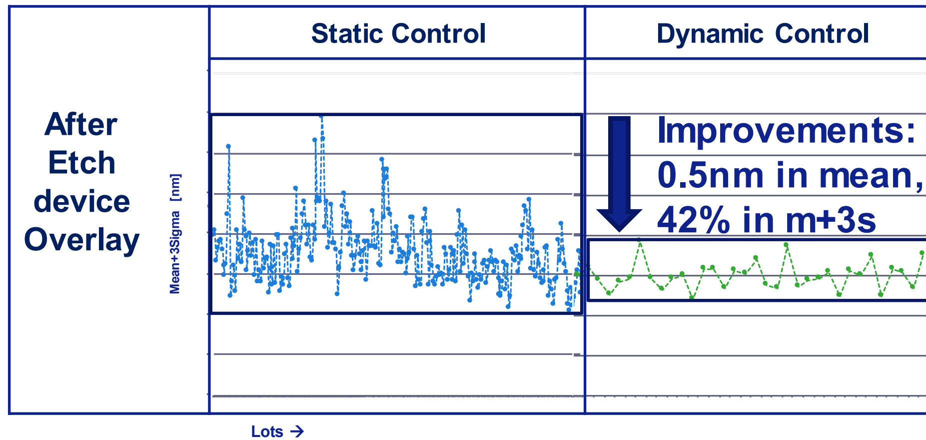

Figure 13. Delta fingerprint after-etch to after-develop varying overtime

3. CONCLUSION

Main contributors to EPE are Local CD error (OPC error, stochastics) and Overlay. With continued shrink (scaling) the local error starts to dominate. SMO can minimize some of this local error and OPC models are improved using machine learning on massive metrology (e-beam) data; however, the remaining local stochastic is still large. In order to meet the overall budget, the allowed overlay margin is reducing to an unprecedented level. We need to do everything possible to improve overlay: improve accuracy in overlay metrology by multi wavelength measurements, address non-linear contribution to overlay calculation model and not only reduce the impact of asymmetry in global level (over the wafer), but should also look in to target level. High order process correction in overlay (using device overlay information): increase in sampling to be mitigated by computational metrology where scanner metro and OV metro are used in conjunction to create dense overlay maps at ADI (can be further boosted by incorporating pre-litho inputs). Feedback control is not always enough and feed-forward is needed for improved overlay performance. Next is to close the gap between on-target overlay and device overlay. Device overlay is addressed by a calibration / validation using real measured data on device after etch (AEI OV).

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