The potential of EUV lithography

Harry J. Levinson*
HJL Lithography, 12508 Radoyka Drive, Saratoga, CA 95070

ABSTRACT

Lithographers are currently unable to generate quality patterning at tight pitches with values of k_1 that are as low as have been achieved routinely using ArF immersion patterning, a situation that is largely due to the continuing pursuit of resists with low exposure doses. As a consequence, multiple patterning may be required to scale to a second node with EUV lithography, which reduces its cost-effectiveness, even if each individual exposure is done with a low exposure dose. Because of process control limitations, such multiple patterning may necessarily be triple or quadruple patterning, rather than double patterning. Processes with reduced line-edge roughness (LER) could be applied to front-end layers, increasing the value of EUV lithography. High-NA EUV lithography is in development, with a number of technical issues requiring solution, but with no apparent show-stoppers.

Keywords: Lithography, EUV, line-edge roughness, LER, high-NA

1. INTRODUCTION

To date, the semiconductor industry has invested billions of dollars on the development of EUV lithography. For example, an early consortium dedicated to the development of EUV lithography, the EUV LLC, involved an investment of more than $270M.[1] Later, consortia such as INVENT[2] and imec invested additional hundreds of millions of dollars into EUV lithographic technology. Companies producing key elements of EUV infrastructure such as mask blanks, inspection tools, resists, and exposure systems have also made significant investments into EUV technology. For a single company that fabricates chips, it has been estimated that a minimum initial capital investment of one billion dollars is needed to start using EUV lithography in high-volume manufacturing (HVM).[3] Whether or not companies realize a positive return on their investments in EUV technology is dependent on the semiconductor industry's ability to extend the technology to future nodes and how much more investment will be required. No insurmountable problems for extensibility have been identified, but several issues need to be confronted, with solutions identified and implemented in order to extend EUV lithography beyond one or two nodes.

2. EXTENDING EUV LITHOGRAPHY SINGLE PATTERNING AT 0.33 NA

2.1 Limitations imposed by stochastics

Lithographers are currently struggling to pattern 32 nm pitch lines and spaces with defect levels sufficiently low to be suitable for HVM.[4] With NA = 0.33, this represents patterning at k_1 = 0.39, which is not particularly aggressive by the standards of optical lithography. It has long been understood that LER limits the patterning quality of tight pitches using EUV lithography, and in recent years there has been an improved understanding of the role of stochastic phenomena, such as resist inhomogeneities and photon shot noise, in limiting EUV lithographic capability.[5] It is well-understood that photon shot noise sets a level for the minimum possible LER. For a given LER requirement, this implies that there is a minimum exposure dose for a process to have suitable yield. Indeed, values of LWR as low as 2.5 nm have been demonstrated with doses ~100 mJ/cm^2.[6] Resist engineering can enable LER that is close to the minimum possible LER set by the dose. For example, the impact of photon shot noise can be reduced with resists that have greater optical absorption at EUV wavelengths[7] and greater quantum efficiency. Critically, resists need to be designed with doses-to-size that are large enough to avoid patterning failures due to photon shot noise. Homogeneity of the individual constituents of resists is also needed. Extending EUV lithography to lower values of k_1 will require considerable improvement in resists over current performance levels, and EUV light source power will need to be increased in order to maintain exposure tool throughput at cost-effective levels.

*hjlevinson@comcast.net

35th European Mask and Lithography Conference (EMLC 2019), edited by Uwe F.W. Behringer, Jo Finders, Proc. of SPIE Vol. 11177, 1117702 · © 2019 SPIE
CCC code: 0277-786X/19/$21 · doi: 10.1117/12.2528446

In an interesting study, the fundamental capabilities of chemically amplified resists were investigated through simulation of "virtual resists," that is, the exploration of performance by performing simulations over a wide range of resist parameters.[8] There were two interesting conclusions from this study. First, throughout the entire parameter space, low values of the local critical dimension uniformity (LCDU) of contact holes could only be achieved at doses of 40 mJ/cm^2 and higher. Second, even at doses of 100 mJ/cm^2 and higher, LCDU was greater than ~2 nm (3σ), suggesting that achieving yield at future nodes may require using something other than conventional chemically amplified resists.

Fortunately, alternatives to chemically amplified resists are being explored. Promising results have been obtained with new materials, such as metal-oxide resists,[9, 10] which are based on radiation chemistries that are substantially different from typical chemical amplification. Metal-oxide imaging materials have two advantages over conventional organic chemically amplified resists. First, incorporation of metals, such as tin, increases the optical absorption at EUV wavelengths, which mitigates photon shot noise. Second, such resists have fewer components than typical chemically amplified resists, which helps to reduce the stochastics contributions to LER of the resist materials. The diameters of the metal-oxide cores, currently estimated to be ~0.7 nm,[11] may need to be reduced in order to meet the LER requirements of future nodes, since the core size sets a fundamental limit for LER. Other alternatives to conventional chemically amplified resists have been proposed, such as multi-trigger resists[12] and Photosensitized Chemically Amplified Resist™ (PSCAR™),[13] but these materials need to be studied in more detail at pitches ≤ 32 nm in order to determine the extent to which they can provide the patterning capability required for future nodes.

2.2 Mask defects

Mask defects have long been recognized as a problem for EUV lithography,[14] and improvements in this area are still needed. Mask blank defects have been reduced substantially in recent years,[15] but the supply of very low defect blanks needs to be increased, particularly if EUV lithography is going to be applied to metal layers, as well as contacts, vias and block masks. It has been noted that chip companies will insert EUV lithography into HVM without ideal mask-defect solutions.[16] HVM-worthy pellicles are also still in development,[17] and this necessitates regular mask qualifications, which adds costs to EUV lithography and increases cycle time. At-wavelength and electron-beam inspection tools are still maturing and will add to the cost of defect inspection. Moreover, direct electron-beam inspection of masks is not a completely satisfactory solution, since such inspection cannot be performed with a pellicle attached. The high costs of EUV light sources and mirror-optics have been barriers to the development of actinic inspection tools, but innovative approaches, such as the use of high-harmonic generation light sources and zone plate optics, have been used to address this problem.[18]

In the absence of pellicles and actinic inspection tools, EUV masks are currently qualified using a combination of direct optical inspection and defect inspection of patterned wafers. The resolution capabilities of optical inspection tools are being exceeded with the dimensions involved with EUV lithography. These problems with mask defects and inspection are already relevant to the first generation of EUV lithography. For future nodes, the problems of resolution and defect detection will grow. Creating defect control solutions at smaller features will need to occur while simultaneously addressing problems not completely solved at earlier nodes.

2.3 Mitigation of mask 3D effects

Mask 3D effects constitute a class of phenomena that has long been recognized,[19] but where greater understanding has been gained in recent years. Heightened attention to mask 3D effects has been driven in large measure by their increased significance at the dimensions of future generations of technology for which EUV lithography is expected to be used. Manifestations of mask 3D effects include dependence of the planes of best focus on pitch,[20] pattern shifts coupled to focus variations,[21] and image blurring.[22] Optimization of the source and mask to mitigate these effects involves a significantly more complex computational situation than encountered in optical lithography, where OPC computation times are already approaching unacceptable levels. Because EUV lithography will be applied to designs with extremely high levels of integration, much faster computational capabilities will be needed.

Sub-resolution assist features (SRAFs) can be used to mitigate mask 3D effects, many of which are manifested as variations through pitch. Recently, the benefits of curvilinear SRAFs and even curvilinear primary features have become recognized.[23, 24] For many years, the difficulties associated with patterning masks with curvilinear features has been the biggest impediment for implementing such types of patterns. However, the recent introduction of multi-beam mask writers[25, 26] makes it much easier to pattern such masks. Development of tools for mask rule checks (MRC) and design rule checks (DRC) has started,[27] and further improvements can be expected to bring them fully to maturation.

The manifestations of mask 3D effects can also be reduced though the use of alternative absorbers[28] and/or multilayer reflectors,[29] but these require long-term development. In addition to having the fundamental characteristic of high absorption, new absorber materials must also meet requirements for etch, clean and repair. There are also constraints on the real part of the absorber's index of refraction, depending upon whether the intention is the fabrication of binary or attenuated phase-shifting masks.[30]

2.4 Process control for EUV lithography

EUV lithography will be applied in HVM at the 7-nm node and beyond, involving processes with very tight pitches. Accordingly, process control capabilities, such as for overlay and critical dimensions, will need to be consistent with the requirements of these pitches. Overlay control will need to be 3.5 nm (3σ) and tighter.[31] Moreover, with EUV lithography there are sources of overlay error, such as mask non-flatness[32] and non-telecentricity,[21] that are not found in optical lithography, and the impact of aberrations on overlay will be greater for EUV than for optical lithography.[33]

Focus control will need to be very tight for future generations of EUV lithography. When using 0.33 NA optics, these tight control requirements are driven primarily by mask 3D effects. In contrast to optical lithography, the focus budget for EUV lithography is determined to a large extent by overlay requirements, because of image placement errors that are a function of defocus. Image blurring due to mask 3D effects also places a constraint on focus, since blurring can be reduced significantly by strongly limiting focus variation.[34] For 0.55 NA EUV lithography, discussed further in Section 4, the Rayleigh depth-of-focus is merely 45 nm. This is only ~1/3 of the Rayleigh depth-of-focus at NA = 0.33. Because the real part of the index of refraction of resist ≈ 1 at λ = 13.5 nm, the full resist thickness will be part of the total focus budget, a situation different from that which occurs in optical lithography.[35] Regardless of which factor is most significant, focus will need to be controlled very tightly for future nodes using EUV lithography.

3. EUV MULTIPLE PATTERNING

Immersion ArF lithography at 1.35 NA has been used in manufacturing for almost a decade, having been extended to additional nodes by the use of multiple patterning. Consequently, it is natural to contemplate a similar extension of EUV lithography. The problems with EUV single patterning described in Section 2 have provided additional impetus for such considerations at larger values of k_1 than the entry point for immersion multiple patterning.

While developing immersion double patterning, technologists began to recognize significant increases in patterning costs due to the increase in the number of process operations, and steps were taken to compensate for these extra costs, including layout modifications and deeper shrinks than the traditional node-to-node 0.7× linear scaling. If we assume that EUV lithography is first used in HVM for processes with 40 nm metal pitches, this implies that the pitch for second generation EUV lithography needs to be < 28 nm if double patterning is required. At such tight pitches, the process control budget needs to be studied in detail.

A typical situation involving multiple patterning is depicted in Fig. 1. Proper processing requires that the block feature overlays the line it is intended to block, while not encroaching on a neighboring line. This process control requirement can be estimated from the following condition for the variation in G:

$$3\sigma_G = \sqrt{OL^2 + \frac{\Delta S^2}{2} + \frac{\Delta B^2}{2}} \tag{1}$$

where *OL* is the overlay variation (3σ), and Δ*S* and Δ*B* represent the variations in the dimensions S and B. In Eq. 1, it is assumed that the total variation is the root sum of squares of the variation of the components. For illustration, consider a situation involving a 20-nm pitch line/space pattern consisting of equal lines and spaces. If we further assume that critical dimensions are controlled to ±15%, and the overlay control is 3.0 nm (3σ), then $3\sigma_G$ = 3.4 nm. Even using $4\sigma_G$ = 4.6 nm as the target for process control in high-volume manufacturing (HVM), it would seem that the level of process control is adequate for using double patterning to fabricate 20 nm pitch line/space patterns. However, due to stochastics, this may not be the case.

The statistics of process control have been changing as stochastics have become more significant. Controlling processes to ±4σ has long been used in high-yield manufacturing. Since processes controlled to this level have 63 ppm failure rates (assuming normal variation), it might seem not possible to yield circuits with billions of transistors. However, it has been possible to yield such large circuits at this level of process control, because occurrences that are out-of-specifications for

parameters such as critical dimensions and overlay do not occur randomly in optical lithography. This is shown schematically in Fig. 2. Over much of the wafer (area A), the relevant process parameters are within specification, while on a different part of the wafer (area B) they are not. In area B, where the out-of-specification conditions occur, there are often multiple locations in which the relevant parameter is out-of-specifications. Thus, devices with billions of transistors can yield even with processes controlled only to ±4σ, because the failures do not occur randomly: chips in area A can yield, while those in area B will likely not.

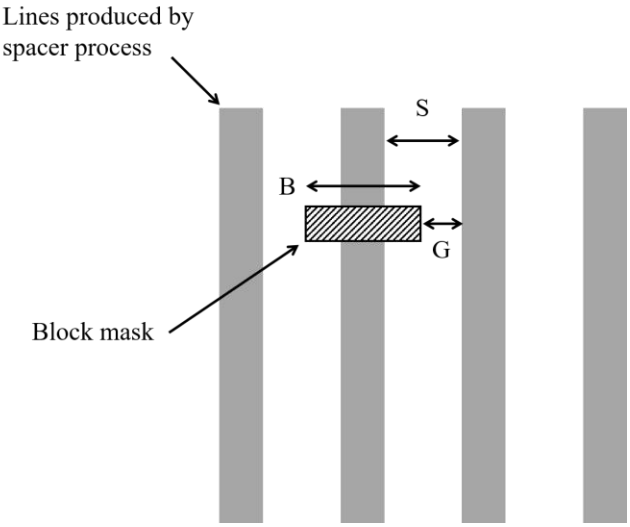

Figure 1. Schematic of block masking for a line-space pattern generated using a spacer process.

In EUV lithography, the situation is different, because of stochastic phenomenon. It has been argued that LER should be added to Eq. 1,[36] resulting in:

$$3\sigma_G = \sqrt{OL^2 + \frac{\Delta S^2}{2} + \frac{\Delta B^2}{2} + LER_S^2 + LER_B^2} \tag{2}$$

Moreover, LER should be included at the 6σ or 7σ level. If LER is only 1.5 nm (3σ), then the "4σ" level of control for G increases to 7.3 nm. This means that the smallest pitch for which double patterning is possible is ~28 nm. At tighter dimensions, self-aligned block masks would be required, leading to triple or quadruple patterning.[37] Since EUV lithography is expected to be on-par with the costs of immersion triple patterning, adding additional EUV exposures is a very expensive proposition.

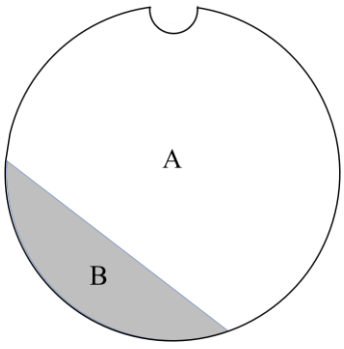

Figure 2. Illustration of non-randomness. For process parameters, such as overlay, values may be within specifications throughout area A of a wafer, while being out of specifications at multiple locations in area B.

It has been argued that the cost of EUV multiple patterning is mitigated because each exposure step can be done at low exposure dose. If the line-space pattern illustrated in Fig. 1 is created using EUV lithography and a spacer process, the linewidth roughness (LWR) will be low, but the line-edge roughness LER remains. Consequently, if low dose resists are used, the resulting LER will increase the minimum pitch which can be patterned using double lithography. Moreover, the throughput advantage of low dose does not scale directly with the dose. Consider the graph in Fig. 3. At 250 W source power (at intermediate focus), the throughput with a resist sensitivity of 20 mJ/cm^2 is slightly more than 50% greater than the throughput with a resist sensitivity of 40 mJ/cm^2. This means that the exposure tool capital cost of double patterning at 20 mJ/cm^2 is about 30% greater than single patterning at 40 mJ/cm^2. For actual double patterning, there are the additional costs of masks, consumables and non-lithographic operations, so double exposure at low dose is a costly solution. It is worth noting that EUV multiple patterning is being discussed for NA = 0.33 because of persistence in targeting EUV lithography at low exposure doses, which prevents single patterning at values of k_1 which are low but consistent with optical resolution. This contrasts with what occurred in optical lithography, where multiple patterning was widely used only after limits were reached for numerical aperture and wavelength reduction, and there were no optical lithographic alternatives to multiple patterning consistent with the laws of physics. Similarly, consideration of multiple patterning with EUV lithography is sensible once limits to numerical aperture and wavelength have been met. Higher numerical aperture for EUV lithography is the topic of the next section.

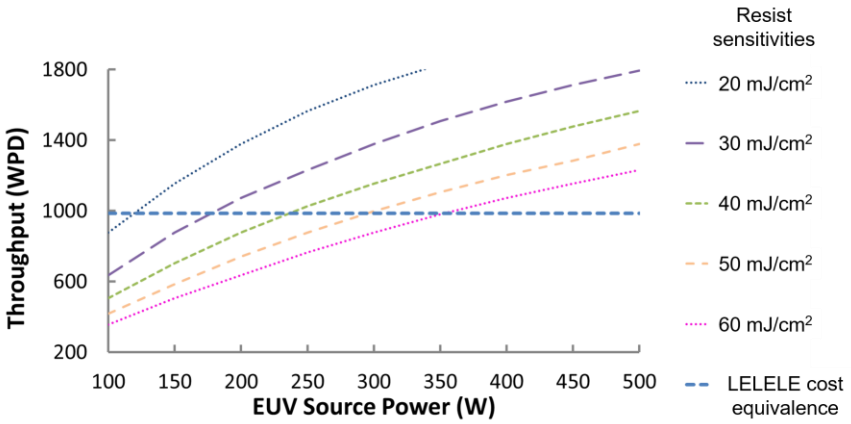

Figure 3. Output per day of a single EUV cluster.[38] This graph was based on assumption of 88% system availability and 75% utilization.

4. HIGH NA EUV LITHOGRAPHY

Prior lithographic technologies, such as i-line, KrF and ArF lithography, have been applied to multiple nodes, primarily through increases in numerical aperture over time. This occurred in ArF optical lithography until a physical limit to numerical aperture was effectively reached. In a similar manner, Zeiss and ASML are developing EUV optics and exposure tools at 0.55 NA. The challenges of fully enabling high-NA EUV lithography have been discussed previously,[15] and a summary is provided in Table 1. The issue of resist stochastics, including photon shot noise, was discussed in Sec. 2.1. It has been argued that high-NA EUV lithography will help to address the problem of stochastics by providing an aerial image with greater acuity. However, this is an expensive solution to the problem of stochastics. It means that the full potential of EUV lithography at NA = 0.33 will be unrealized. To parallel what occurred in optical lithography, single patterning at NA = 0.33 down to $k_1 \approx 0.3$ (24 nm pitch) is needed, followed only then by the introduction of high numerical aperture. Finally, multiple patterning would be used after a practical limit to NA has already been reached.

At NA = 0.55, the Rayleigh depth-of-focus will be only 45 nm. It will be very challenging to control focus to this level. To reduce the impact of mask 3D effects, these high-NA systems have anamorphic lenses with reduced field sizes.[39] This will have an impact on the productivity of high NA tools, particularly for fabricating dies too large to fit into a single reduced-size exposure field (necessitating stitching), thereby adding to the return-on-investment challenge. New

generations of lithographic technology have often required construction of new fabs that can support the facilities requirements of new tool sets. While the technical issues are straightforward, this will require additional investments. Changes of numerical aperture also necessitate acquisition of new tools for mask making, such as AIMS tools. Finally, realization of the full theoretical resolution potential of 0.55 NA optics will require control of polarization. Coupled with the small depth-of-focus at NA = 0.55, there would be value in having variable numerical aperture for future EUV exposure tools. High NA EUV exposure tools are also expected to cost considerably more than current 0.33 NA tools, leading to additional return-on-investment challenges. All of these should be viewed as problems that soluble – there are no apparent show-stoppers currently recognized for high-NA EUV lithography.

Table 1. Technical and cost challenges for enabling 0.55 NA EUV lithography

1.	Resists meeting resolution requirements, with low levels of defects from stochastic phenomena and pattern collapse
2.	Light sources that can support requisite photon shot noise and productivity requirements
3.	Solutions for meeting small depths-of-focus at 0.55 NA
4.	Solutions for stitching large dies
5.	New fabs capable of supporting high NA exposure tools
6.	Mask making and metrology infrastructure
7.	Polarization control for maintaining high contrast at 0.55 NA
8.	Cost of high-NA EUV exposure tools

5. SUMMARY

There is good potential for the semiconductor industry to get a positive return-on-investment for EUV lithography by extending the technology to multiple nodes. Cost-effective extension will require that stochastic-induced resist process variations, including defects, be controlled to adequate levels. This may necessitate development of resists that are very different from the types of chemically amplified resists that have been used in leading-edge lithography for decades. Sufficiently powerful light sources will be needed to bring photon shot noise to acceptable levels without excessively reducing exposure tool throughput. Multiple patterning can be used to shrink pitches further, but this makes sense only after EUV lithography has been extended to a maximum NA. At that point, triple or quadruple patterning will be required for line/space patterns, because edge pattern placement errors necessitate self-aligned block masks. High numerical aperture EUV lithography is undergoing development and offers a useful path for extending EUV lithography, once basic technical issues associated with the new technology are addressed.

REFERENCES

[1] S. Wurm, “The EUV LLC: An Historical Perspective,” in *EUV Lithography*, ed. V. Bakshi, SPIE Press (2018).

[2] J. G. Ryan, D. Back, G. Denbeaux, F. Goodwin, J. Hartley, R. Housley, K. Kemp, K. Kimmel, B. LaFontaine, J. Mackey, A. Ruddack, M. D. Tittnich, O. Wood and P. Naulleau, “EUV Lithography Programs at Albany Nanotech,” EUVL Symposium (2006)

[3] http://semimd.com/blog/2016/11/28/high-na-euv-lithography-investment/

[4] R-H. Kim, O. Wood, M. Crouse, Y. Chen, V. Plachecki, S. Hsu, and K. Gronlund. "Application of EUV resolution enhancement techniques (RET) to optimize and extend single exposure bi-directional patterning for 7nm and beyond logic designs," Proc. SPIE Vol. 9776, p. 97761R (2016).

[5] P. De Bisschop, "Stochastic effects in EUV lithography: random, local CD variability, and printing failures," *Journal of Micro/Nanolithography, MEMS, and MOEMS* 16, no. 4 (2017): 041013.
[6] T. Gädda, N. D. Luong, M. Laukkanen, K. Karaste, O. Kähkönen, E. Kauppi, D. Kazazis, Y. Ekinci, and J. Rantala, "Advanced EUV negative tone resist and underlayer approaches exhibiting sub-20nm half-pitch resolution," Proc. SPIE Vol. 10960, p. 109600B (2019).
[7] R. L. Brainard, P. Trefonas, J. H. Lammers, C. A. Cutler, J. F. Mackevich, A. Trefonas, and S. A. Robertson. "Shot noise, LER, and quantum efficiency of EUV photoresists," Proc. SPIE Vol. 5374, pp. 74-86 (2004).
[8] M. D. Smith, J. Biafore, and C. Fang. "Optimization of a virtual EUV photoresist for the trade-off between throughput and CDU," Proc. SPIE Vol. 8682, p. 868203 (2013).
[9] V. M. Blanco Carballo, J. Bekaert, M. Mao, B. Kutrzeba Kotowska, S. Larivière, I. Ciofi, R. Baert et al., "Single exposure EUV patterning of BEOL metal layers on the IMEC iN7 platform," Proc. SPIE Vol. 10143, p. 1014318. (2017).
[10] W. D. Hinsberg and S. Meyers. "A numeric model for the imaging mechanism of metal oxide EUV resists," Proc. SPIE Vol. 10146, p. 1014604 (2017).
[11] R. Maas, M. van Lare, G. Rispens, and S. F. Wuister. "Stochastics in extreme ultraviolet lithography: investigating the role of microscopic resist properties for metal-oxide-based resists," *Journal of Micro/Nanolithography, MEMS, and MOEMS* 17, no. 4 (2018): 041003.
[12] Y. Vesters, A. McClelland, D. De Simone, C. Popescu, G. Dawson, J. Roth, W. Theis, G. Vandenberghe, and A. PG Robinson. "Multi-trigger resist patterning with ASML NXE3300 EUV scanner," Proc. SPIE Vol. 10583, p. 1058308 (2018).
[13] C. Q. Dinh, S. Nagahara, G. Shiraishi, Y. Minekawa, Y. Kamei, M. Carcasi, H. Ide et al. "Calibrated PSCAR stochastic simulation," Proc. SPIE Vol. 10957, p. 109571O (2019).
[14] K. B. Nguyen, A. K. Ray-Chaudhuri, R. H. Stulen, K. Krenz, L. A. Fetter, D. M. Tennant, and D. L. Windt. "Printability of substrate and absorber defects on extreme ultraviolet lithographic masks." *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 13, no. 6 (1995): 3082-3088.
[15] S-S. Kim, R. Chalykh, H. Kim, S. Lee, C. Park, M. Hwang, J-O. Park et al. "Progress in EUV lithography toward manufacturing," Proc. SPIE Vol. 10143, p. 1014306 (2017).
[16] M. Preil and J. W. Westphal, "Open issues in mask technology as EUV enters high volume manufacturing," Proc. SPIE Vol. 11178, p. 111780C (2019).
[17] B. Turkot, S. Carson, and A. Lio. "Continuing Moore's law with EUV lithography," In *Electron Devices Meeting (IEDM), 2017 IEEE International*, pp. 14-4. IEEE, 2017.
[18] J. Na, D. Lee, C. Do, H. Sim, J. Lee, J. Kim, H. Seo, H. Kim, and C. U. Jeon. "Application of actinic mask review system for the preparation of HVM EUV lithography with defect free mask," Proc. SPIE Vol. 10145, p. 101450M (2017).
[19] P-Y. Yan, "Understanding Bossung curve asymmetry and focus shift effect in EUV lithography." Proc. SPIE Vol. 4562, pp. 279-288 (2002).
[20] T. Last, L. de Winter, P. van Adrichem, and J. Finders. "Illumination pupil optimization in 0.33-NA extreme ultraviolet lithography by intensity balancing for semi-isolated dark field two-bar M1 building blocks." *Journal of Micro/Nanolithography, MEMS, and MOEMS* 15, no. 4 (2016): 043508.
[21] S. Raghunathan, O. R. Wood, P. Mangat, E. Verduijn, V. Philipsen, E. Hendrickx, R. Jonckheere et al. "Experimental measurements of telecentricity errors in high-numerical-aperture extreme ultraviolet mask images." *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* 32, no. 6 (2014): 06F801.
[22] J. Finders, E. van Setten, P. Broman, E. Wang, J. McNamara, and P. van Adrichem, 2017, October, "EUV source optimization driven by fundamental diffraction considerations," Proc. SPIE Vol. 10450, p. 104500C (2017)
[23] K. Hooker, A. Kazarian, X. Zhou, J. Tuttle, G. Xiao, Y. Zhang, and K. Lucas. "New methodologies for lower-K1 EUV OPC and RET optimization" Proc. SPIE Vol. 10143, p. 101431C (2017).
[24] R. Pearman, J. Ungar, N. Shirali, A. Shendre, M. Niewczas, Leo Pang, A. Fujimura, "How curvilinear mask patterning will enhance the EUV process window: a study using rigorous wafer+mask dual simulation," Proc. SPIE 11178, p. 1117809 (2019).
[25] E. Platzgummer, "Progress report of MBMW-101 and introduction of the 2nd generation multi-beam mask writer," presented at Photomask Japan 2019.

[26] H. Matsumoto, H. Kimura, T. Tamura, and K. Ohtoshi, “Multi-beam mask writer MBM-1000,” presented at Photomask Japan 2019.
[27] B. Su, O. Syrel, M. Pomerantsev, K. Hagiwara, R. Pearman, L. Pang, and A. Fujimara. "Simulation-based MDP verification for leading-edge masks," Proc. SPIE Vol. 10454, p. 1045409 (2017).
[28] O. Wood, S. Raghunathan, P. Mangat, V. Philipsen, V. Luong, P. Kearney, E. Verduijn et al. "Alternative materials for high numerical aperture extreme ultraviolet lithography mask stacks," Proc. SPIE Vol. 9422, p. 94220I (2015).
[29] O. Wood, K. Wong, V. Parks, P. Kearney, J. Meyer-Ilse, V. Luong, V. Philipsen et al, "Improved Ru/Si multilayer reflective coatings for advanced extreme-ultraviolet lithography photomasks," Proc. SPIE Vol. 9776, p. 977619 (2016).
[30] V. Philipsen, V. Luong, K. Opsomer, L. Souriau, E. Hendrickx, C. Detavernier, A. Erdmann, P. Evanschitzky, C. Laubis, P. Hoenick, and V. Soltwisch, “Mask absorber development to enable next-generation EUV Lithography,” Proc. SPIE Vol. 11178, p. 111780F (2019)
[31] https://irds.ieee.org/
[32] M. Chandhok, S. Goyal, S. Carson, S-J. Park, G. Zhang, A. M. Myers, M. L. Leeson et al. "Compensation of overlay errors due to mask bending and non-flatness for EUV masks," Proc. SPIE Vol. 7271, p. 72710G (2009).
[33] Y. Chen, L. Liebmann, L. Sun, A. Gabor, S. Zhao, F. Luo, O. Wood et al. "Holistic analysis of aberration induced overlay error in EUV lithography," Proc. SPIE Vol. 10583, p. 105830D (2018).
[34] M. Burkhardt, A. De Silva, J. Church, L. Meli, C. Robinson, and N. Felix, "Investigation of mask absorber induced image shift in EUV lithography," Proc. SPIE Vol. 10957, p. 1095710 (2019).
[35] W. H. Arnold and H. J. Levinson. "Focus: the critical parameter for submicron optical lithography: part 2." Proc. SPIE Vol. 772, pp. 21-35 (1987).
[36] A. H. Gabor, A. C. Brendler, T. A. Brunner, X. Chen, J. A. Culp, and H. J. Levinson. "Edge placement error fundamentals and impact of EUV: will traditional design-rule calculations work in the era of EUV?," *Journal of Micro/Nanolithography, MEMS, and MOEMS* 17, no. 4 (2018): 041008.
[37] S. Decoster, F. Lazzarino, D. Vangoidsenhoven, V. M. B. Carballo, A-H. Tamaddon, E. Kesters, and C. Lorant, "Exploration of EUV-based self-aligned multipatterning (SAMP) options targeting pitches below 20nm," Proc. SPIE Vol. 10960, p. 109600L (2019).
[38] E. Hosler, “EUV Lithography: The Next Generation,” presented at Semicon West (2018).
[39] J. van Schoot, E. van Setten, K. Troost, F. Bornebroek, R. van Ballegoij, S. Lok, J. Stoeldraijer et al. "High-NA EUV lithography exposure tool progress (Conference Presentation)" In *International Conference on Extreme Ultraviolet Lithography* Vol. 10809, p. 108090Z (2018).