Crossing the Divide Between Lithography and Chip Design

William H. Arnold[1], J. Fung Chen[2], & Kurt E. Wampler[2]
1 ASML TDC, Tempe, AZ
2 ASML Masktools, Santa Clara, CA

1.0 Abstract

0.7X reduction every two years, as required by Moore's Law, has increased the emphasis on low k1 imaging. Low k1 is a way to extend each wavelength one node (e.g., 193 nm to 65 nm, 157 to 45 nm).

However, with low k_1 imaging, a significant divide opens between the desires of the chip designer and the realities of lithographic reproduction. As k_1 decreases from the safe and comfortable 0.8 value enjoyed in the 1980s, to the more stringent 0.5 adopted in production in the 90s, lithographers had to beg designers to let them do line biasing and place hammerheads at the ends of gates in order to compensate for simple proximity effects like iso-dense bias and line end shortening. Now, in the new millenium, many chip makers have to develop processes that work below 0.4 k_1, which brings new tensions between the designer and the lithographer in the forms of design rule restrictions, 2D OPC, forbidden pitches, phase assignments, double exposure decompositions, etc.

What can be done to cross this divide between chip design and lithography, as will be required to push k_1 to its limit and thus achieve the ultimate in scaling allowed by optics, is the subject of this paper.

2.0 Introduction

As optical lithography approaches the limits of resolution defined by Rayleigh's equation, $R = k_1\lambda/NA$, it becomes increasingly difficult to print arbitrary circuit patterns with the dimensional fidelity required by chip designers. Lithography tool suppliers have increased numerical aperture, NA, and have developed optical systems for shorter wavelengths, λ, to enable IC manufacturers to continue to scale CMOS transistors. However, these improvements are not enough to continue the 0.7X reduction every two years required by Moore's Law. Thus increasing emphasis is placed on low k_1 imaging technologies.

Resolution = process factor K_1 x wavelength / NA (half pitch)

Method:	NA / process factor K_1	365 nm i-line	248 nm KrF	193 nm ArF	157 nm F2
	0.65	0.63→ 0.80	0.63→ 0.9?	0.70 → 0.9?	
Scanner, no OPC	0.60	335nm	235→185nm		
Conventional sigma 0.7 + simple OPC	0.50	280nm	195→155nm	155→105nm	110→ 85nm
annular + 2D OPC	0.40		175→125nm	125→ 85nm	90→ 70nm
Strong PSM (CPL) or Double dipole : DET	0.30		120→ 90nm	90→ 65nm	70→ 50nm
No image contrast "brick wall"	< 0.25	140 nm	100→ 75nm	75→ 55nm	55→ 45nm

Figure 1: Resolution extension of optical lithography - increase NA, decrease wavelength, go to lower k_1.

Design, Process Integration, and Characterization for Microelectronics, Alexander Starikov,
Kenneth W. Tobin, Jr., Editors, Proceedings of SPIE Vol. 4692 (2002) © 2002 SPIE · 0277-786X/02/$15.00

3.0 Various challenges for low k_1

There are various challenges facing IC makers going to lower k_1. First, there are design rule restrictions that include angled features, minimum pitch, gate and contact hole size, forbidden pitches, corner rounding and line-end shortening. Model based OPC (2D and 3D) is of increasing importance. New challenges include dipole decomposition and model calibration (imaging, resist). Modeling, fabrication, and qualification of different mask types (including binary, low and high T% att PSM, strong PSM + trim and CPL) is a central topic to the whole economics of the IC business. Modeling and achieving various illumination conditions (including conventional, annular, quadrupole, dipole and optimized solutions based on mask spectral content) will be important techniques to squeeze the most from the optics.

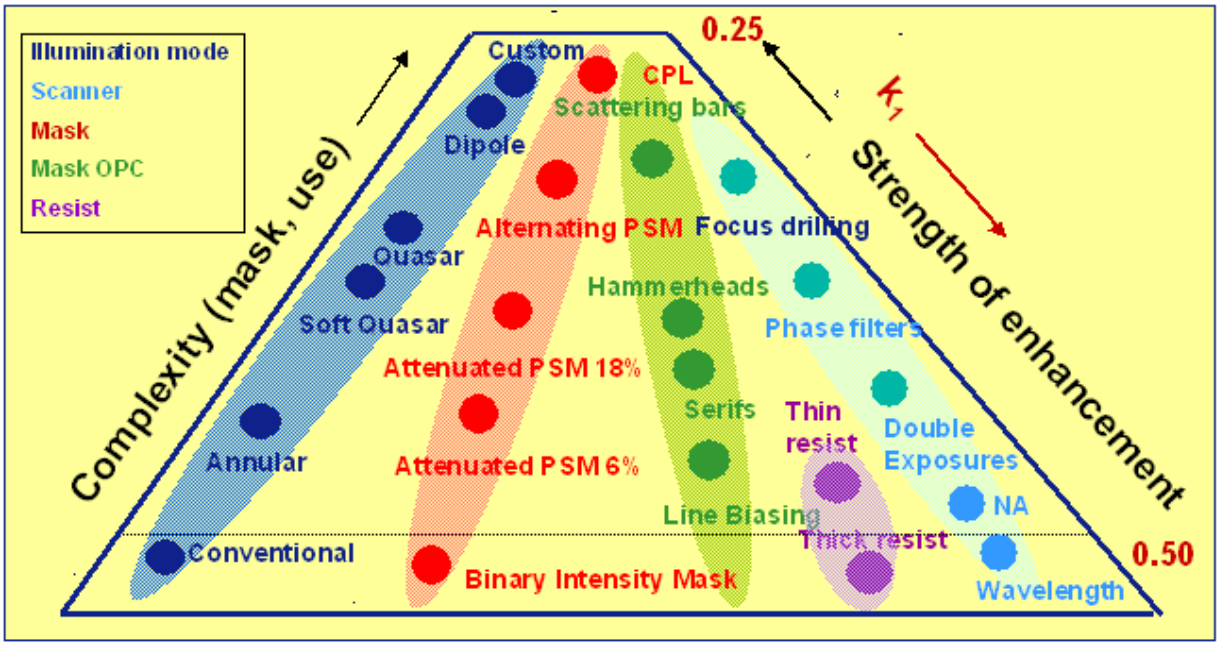

Figure 2: Indicates various low k_1 enhancements possible through improvements to illumination, mask, OPC, resist and scanner technology (1)

Finally, thin film imaging is required due to DOF and resist aspect ratio limitations. Resist coupling at very high NA, sufficient etch resistance in various applications, and ultraplanar processes for small UDOF will be key challenges for resist chemists and process engineers.

4.0 Forbidden pitch

As lithography pushes to 100 and below, two-beam imaging techniques can best maintain sufficient depth of focus (DOF). However, two-beam causes severe proximity effects. Due to these large proximity effects, some pitches may be forbidden in order to overlap process windows with adequate process latitude. In addition to loss of overlapping process latitude for certain pitches, each pitch will sample different portions of the lens. This implies that certain aberrations will cause loss of process window. The type of resist further exacerbates the loss of process window. The process window for a resist is typically optimized for one pitch. In order to optimize the overlapping process window, the reticle enhancement should be applied such that the enhancement causes each pitch to emulate the optimized resist pitch. Therefore, it becomes extremely important to understand the exact topology of the various pitches on the full chip design for specified imaging conditions (2).

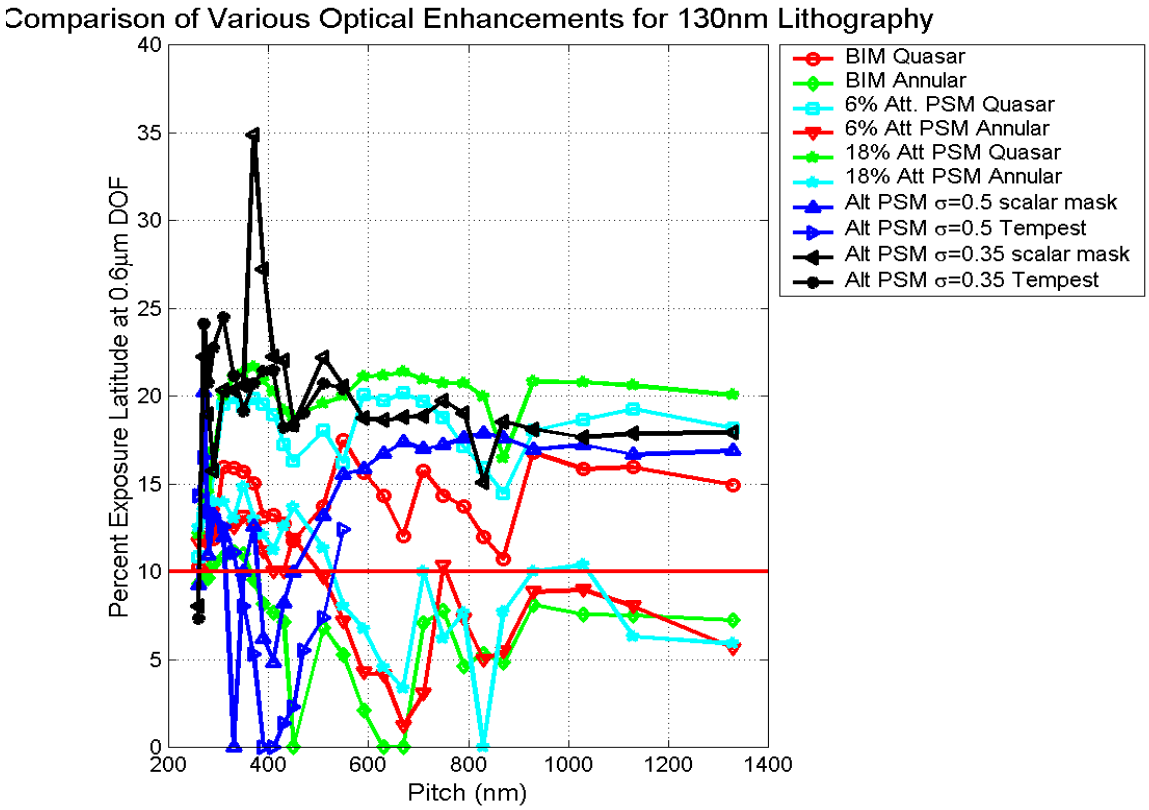

Figure 3: Forbidden pitches limit the exposure latitude (2)

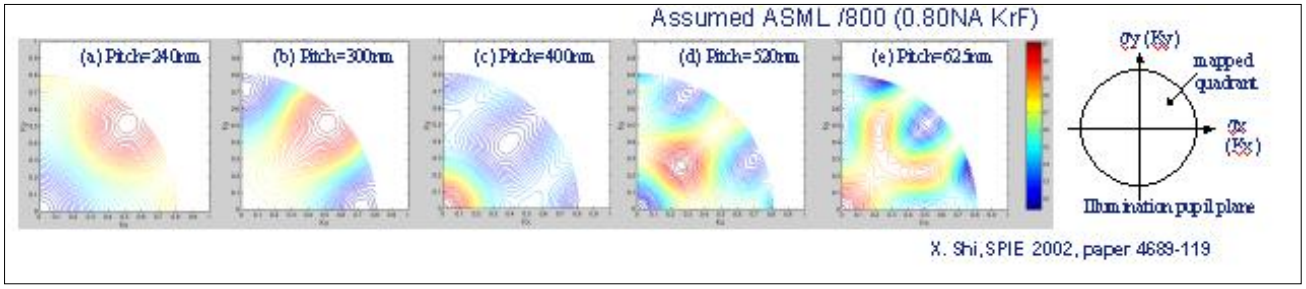

Figure 4: Forbidden pitch is related to illumination – it can be pre-determined for layout optimization (3)

In Figure 4, an example of mapping the spectral content of masks to look for forbidden pitches is shown. 110 nm lines on 5 different pitches are simulated using a 0.80 NA KrF scanner (3). Red log-slope contour lines indicate most desirable illumination source points while the blue ones are undesirable ones. From the five feature pitches investigated, a typical quasar or annular illumination would be a good choice for 240 nm (a) & 300 nm (b) and can be reasonable for 520 nm (d) & 625 nm (e). Neither, however, is a desirable choice for 400 nm pitch (c).

5.0 Optical Proximity Correction (OPC)

Rule based OPC was effective for features larger than 130 nm. Model based OPC is needed for smaller geometries because of stronger proximity effect AND tighter requirements for CD control. The consequences are that both computation time and mask writing data volume are increasing.

6.0 Diagonal Features

Diagonal features are particularly difficult to image with QUASAR illumination due to the reduction in image contrast. Designers will have to avoid diagonal features on layers requiring the tightest resolution, or relax the feature size and pitch.

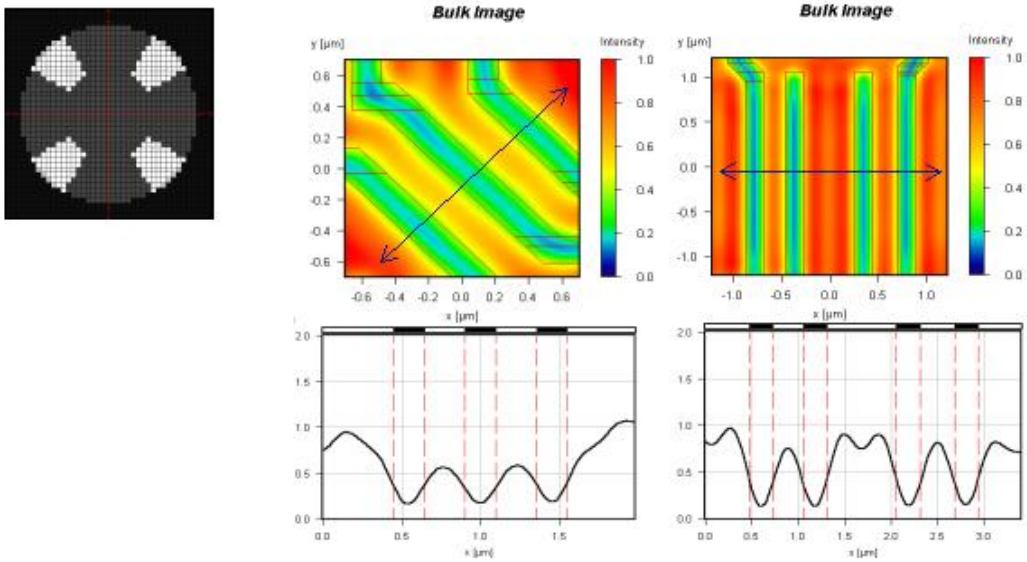

Figure 5: ASML Quasar Illumination enhances H-V features but a 20% area penalty is expected for 45-degree features

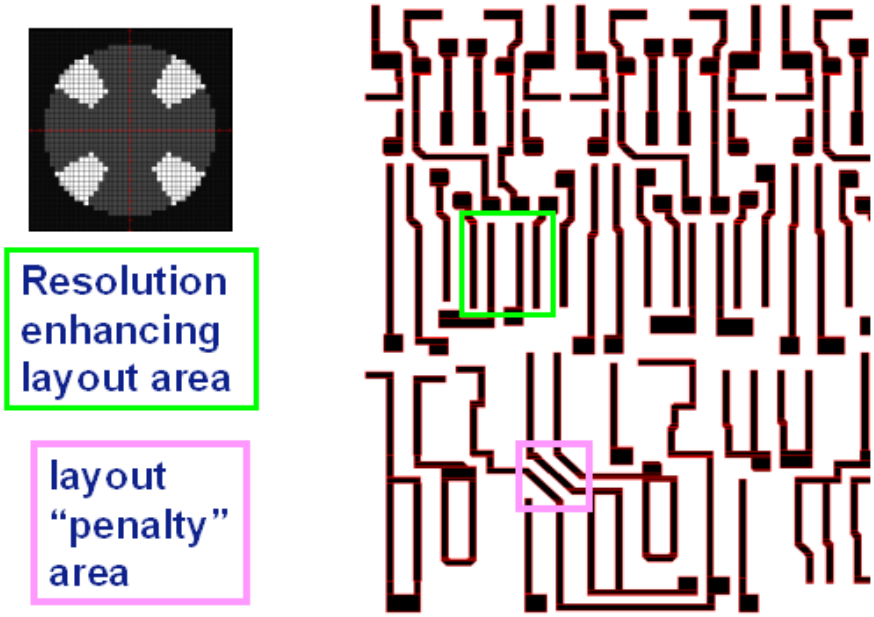

Figure 6: Layout optimization with Quasar Illumination

7.0 Gate Mask

Three low k_1 imaging solutions proposed for poly gate masks at the 65nm node are Alternating PSM (AltPSM) (a double mask exposure solution (3)), Double Dipole (also a double mask exposure solution (4)) and Chromeless Phase Lithography (CPL) (a one mask solution (5)). Each has its own design implementation challenges. Double exposures, using two masks superimposed on one layer, or two exposures of the same mask at different illumination conditions, are useful to overcome resolution limits or proximity effects such as forbidden pitch.

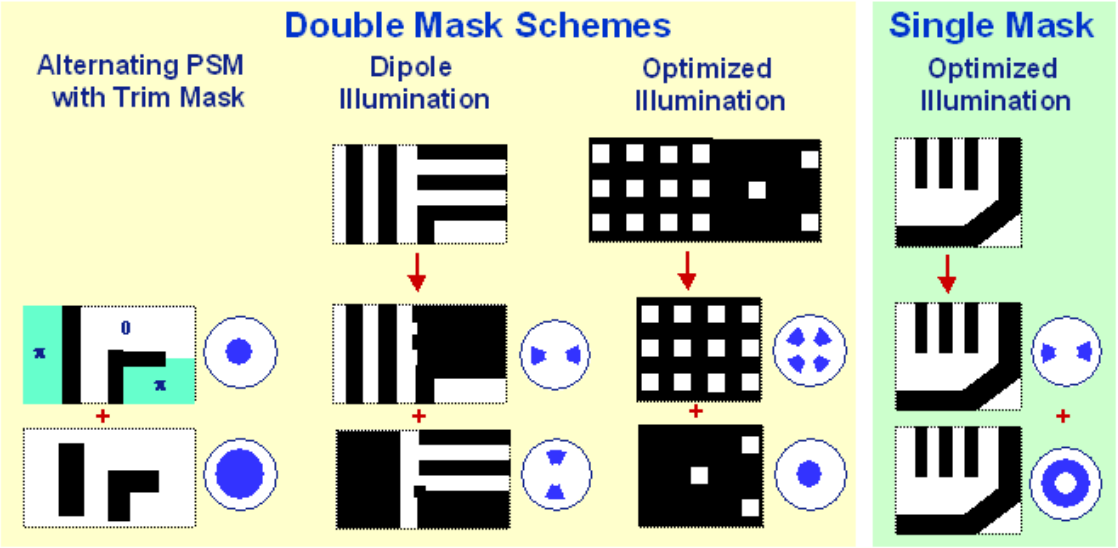

Figure 7: k_1 Reduction using Double Exposure

7.1 Double Dipole

Double dipole (4) is interesting because it enables the imaging of smaller GR (logic-ASIC) devices using binary chrome masks, enables ArF tools to address the 65 nm node and allows chipmakers to stay on their technology roadmap with reasonable mask costs and cycle time. It is not being used now because the double exposure technique means lower productivity and it is not yet a complete solution. What is missing:

- decomposition solution/rule - decomposition algorithms incorporate critical DD imaging knowledge and restrictions (e.g., forbidden pitches);
- full chip software capability - full chip SW which run decomposition algorithms and executes DRC;
- process/tool optimization learning not mature.

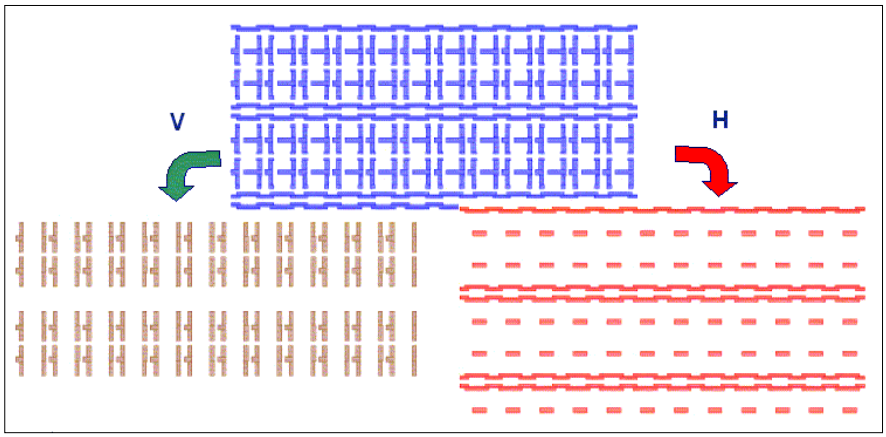

Figure 8:Dipole Mask Decomposition

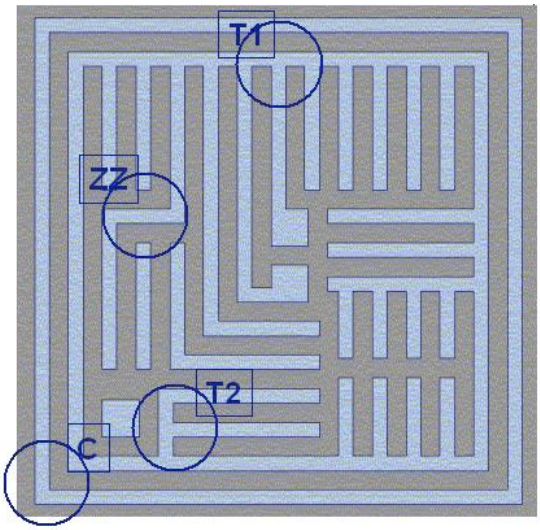

Figure 9: Double Dipole: 2-D test structure

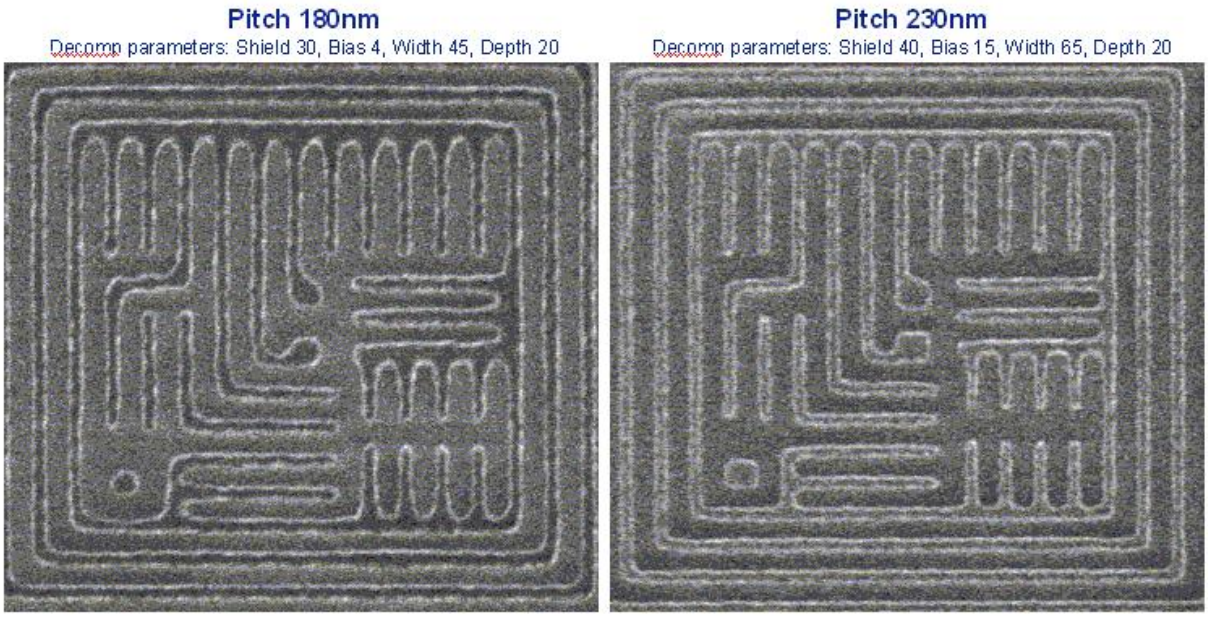

Figure 10: Double Dipole: 70nm Target CD with 193 nm, 0.75 NA Using Binary Chrome Masks *(180 & 230nm pitch examples)* (reference 4)

7.2 Alt PSM

Alternating phase shifting masks are widely used to improve gate resolution and CD control in logic devices. However, alt PSM has several negative aspects. First, as commonly practiced, alt PSM is a double mask exposure technique, with one phase mask and one trim mask, which is undesirable due to the loss in scanner throughput. Mask making is difficult due to the immaturity of phase mask fabrication, inspection, and repair. Many IC businesses can't afford the added cost and cycle time associated with phase masks. A further problem with alt PSM is that, while simple to shrink the gate width, one can't arbitrarily shrink the pitch as well, due to overlay and layout limitations. However, due to the availability of layout software from several suppliers, alt PSM is the strongest contender for volume logic production at 65nm.

7.3 Chromeless Phase Lithography (CPL)

CPL (5) is a phase shifting technique that combines both phase and chrome structures on a single mask. It combines the resolution of alt PSM with the simplicity and high throughput of binary masks. Its applicability to several mask layers - active, contacts, interconnect, as well as gate layer - makes it an attractive candidate for further development. However, layout software and fabrication technology for CPL are still very immature.

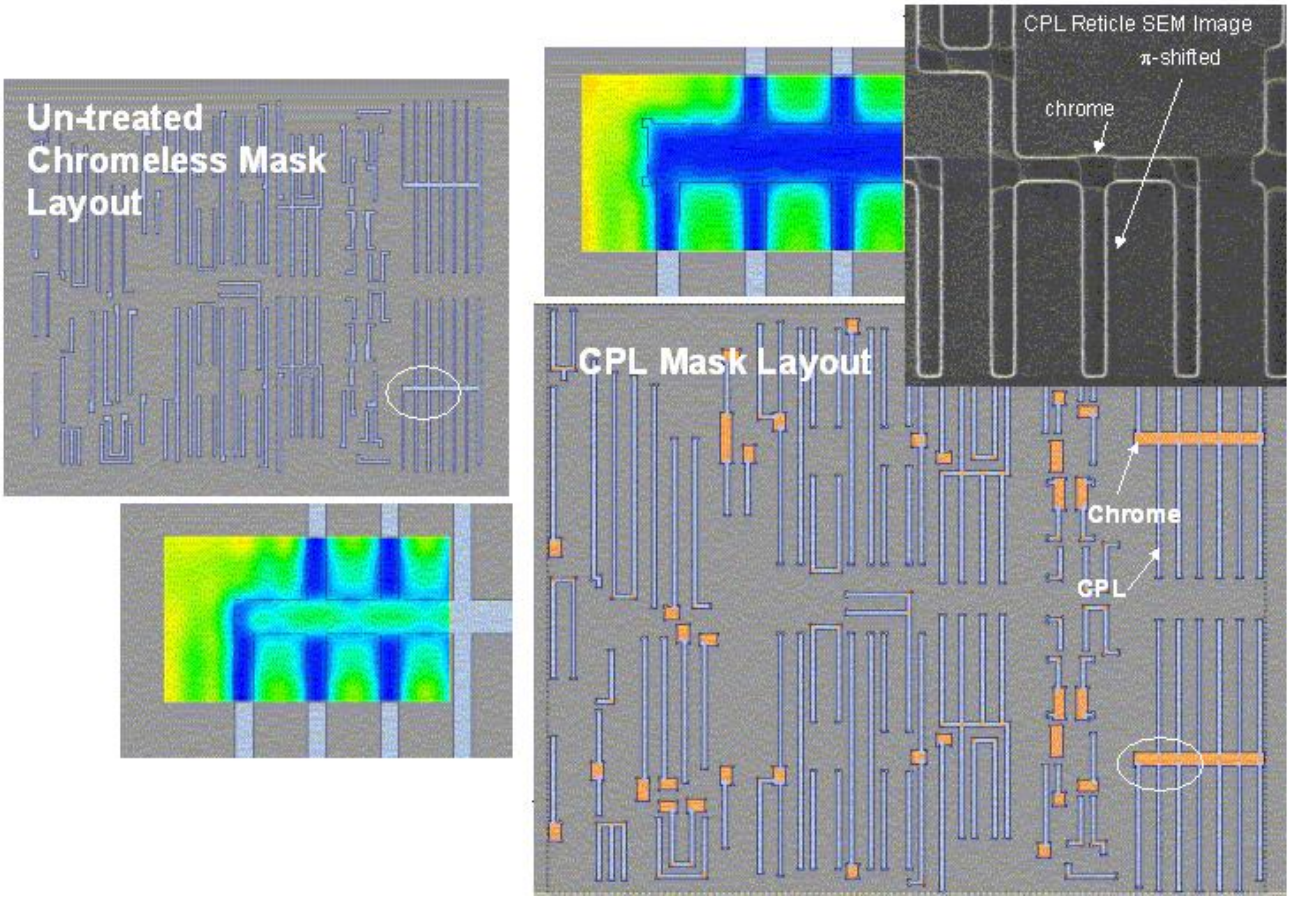

Figure 11: An example of CPL Structure Layout for a logic gate level (5).

8.0 Innovative Low k1 Imaging Solutions Required for Contact / Via Masks

Very low image modulation at low k1 makes it difficult to form acceptable resist patterns on the wafer. Low k1 imaging solutions are available for repeating (DRAM or SRAM) dense contact / via arrays - for example, optimization of the illumination pupil.

Randomly off-grid, dense contact / via arrays are the most challenging. Super high NA (0.85NA or higher) can offer relief. Design rule restriction is likely to be necessary. Automated multiple mask exposure solutions need to be developed. Low k1 imaging friendly contact / via mask layout will be a key enabler for the 65nm node.

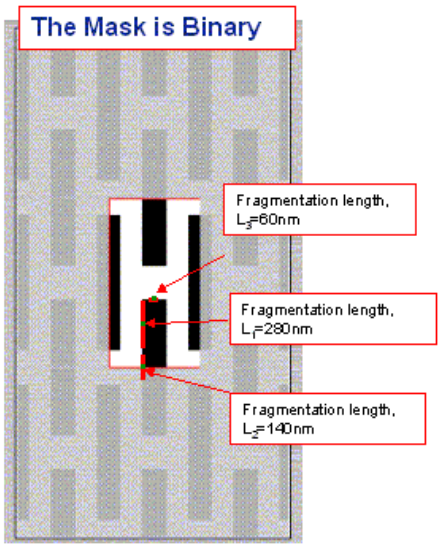

Figure 12: Example of Illumination Optimization

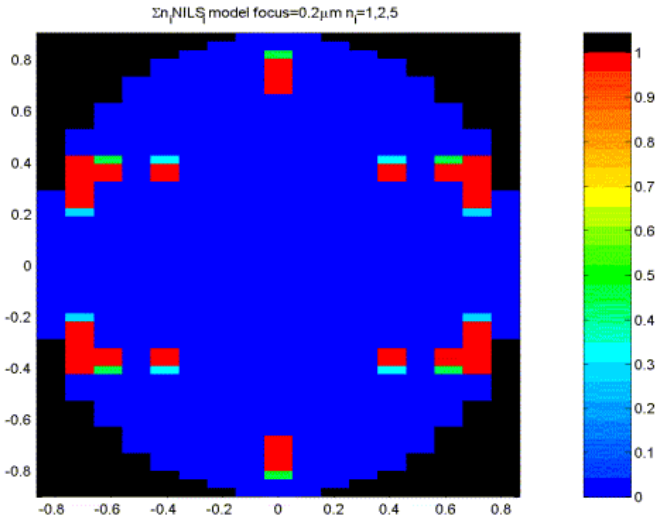

Figure 13: Optimized Pupil for NA = 0.74

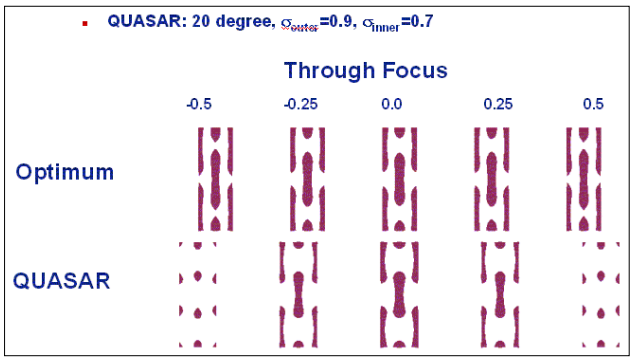

Figure 14: Optimized Pupil vs. Quasar

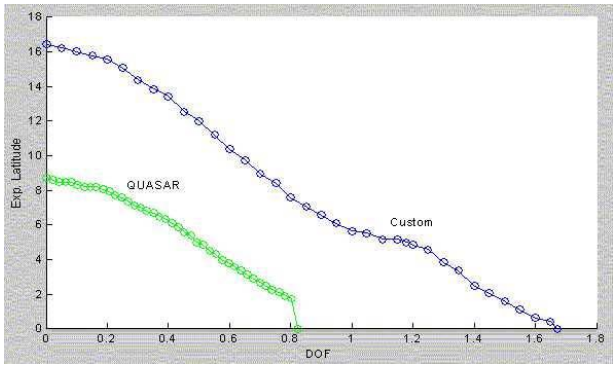

Figure 15: Process Window Comparison - Quasar vs. Optimized Pupil

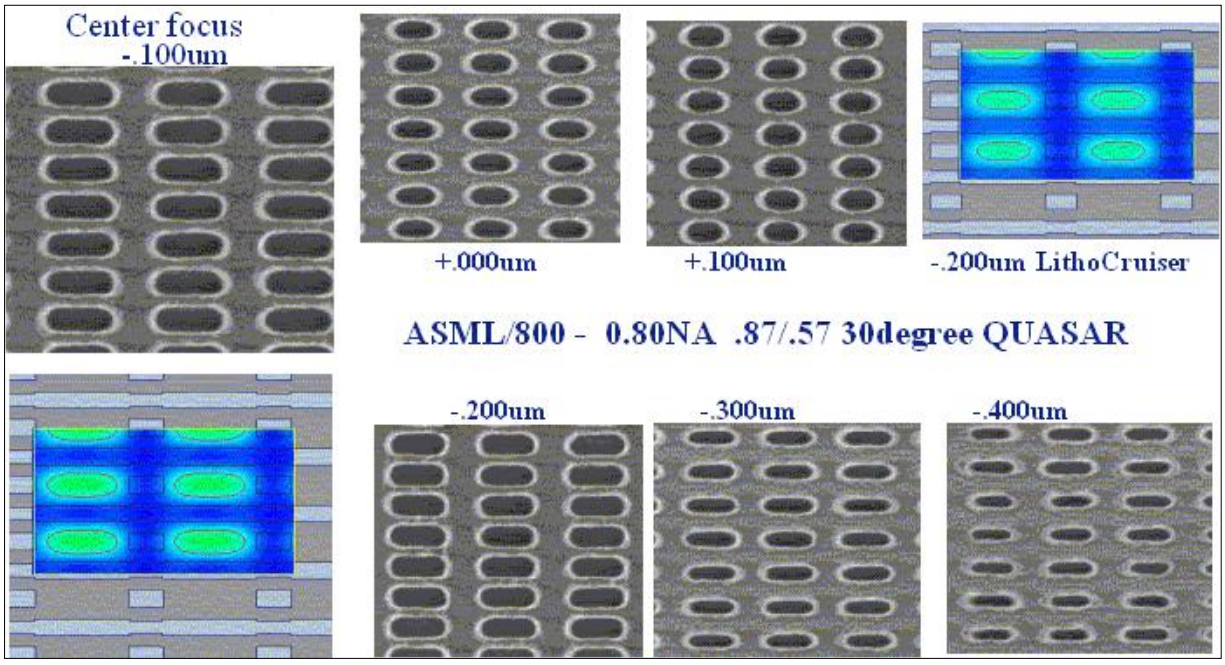

Figure 16: DRAM CAP Layer Imaging at 220nm Pitch (k_1=0.355) CPL Imaging (5)

9.0 How best to implement Low k1 Imaging Solutions

Circuit designers prefer the traditional approach. There is no need to know anything about low k1 imaging lithography, but ask for the following: a given set of reasonable design rules that conforms with low k1 imaging requirements, a full design rule checking (DRC) tool that is trustworthy and fast, and information regarding the expected resulting on-wafer linewidths, tolerances, and across-chip and across-wafer linewidth variation.

However, this approach can cause unacceptable penalties in terms of layout density, compromised imaging, and lower wafer yield. To take full advantage of low k1 imaging, the circuit designer must assume a greater level of responsibility during mask layout in order to achieve greater layout density and high device yield potential.

Simple minimum width and minimum space rules are no longer sufficient to express what layout and circuit designers need to know. The design rules must accurately describe what can be built, and prohibit layout configurations that won't image well or won't yield. Design rules should include the necessary information to enable accurate litho simulation.

10.0 Choice of Photomask Technology

The type of photomask is now tightly coupled to the stepper or scanner. The photomask technology and OPC treatment need to be simultaneously optimized with the illumination pattern and exposure settings. Dry etch technology and e-beam imaging may be needed for managing MEEF, maintaining tight CD variance, and providing satisfactory corner sharpness. Various phase-shifting mask technologies impose their own characteristic restrictions on layout design. Decomposing the layout into two masks can help avoid forbidden pitches, and can make it possible to use directional off-axis illumination (such as dipole).

	k_1(gate)	k_1 (contact)	k_1 (trench)	k_1(1/2 pitch)
BIM	0.41	0.60	0.55	0.43
6% (T)-attPSM	0.35	0.51	0.46	0.43
18% T-attPSM	0.32	0.45	0.41	0.43
CPL	0.28	0.35 ?	0.33	0.30?
DF-AltPSM	0.28		?	0.85

Figure 17: *Estimated* k_1 limits using advanced optical extension masks: Logic - single exposure

BIM: Binary Intensity Mask

6% (T)-attPSM: 6% transmission, (Ternary), attenuated PSM

18% T-attPSM: 18% transmission, Ternary, attenuated PSM

CPL: Chromeless Phase Lithography

DF-AltPSM: Dark Field, double exposure, alternating PSM

Advanced OAI + chrome SB OPC assumed to be used for all masks

11.0 Choice of Layout Design Practices for low k1

Lithographers recommend that designers use rectilinear design rules and abandon diagonal lines for critical resolution layers. If possible, align critical features in one direction. Use a carefully gridded layout, where the grid is chosen to avoid forbidden pitches, and permit only a selected number of line widths. Avoid the introduction of gratuitous edge jogs (such as might be introduced by biasing poly over active). Validate each cell layout with accurate litho simulation that includes focus and exposure variation.

12.0 Breaking Down Communication Barriers

Foundries and captive fabs need to disclose more and better information to designers about process sensitivities and yield killers. They need to work with cell library and design IP providers as well as design houses to validate layouts and ensure that they will scale for several technology nodes before requiring re-layout. Foundries could offer tighter design rules if the designs to be made are lithography-friendly.

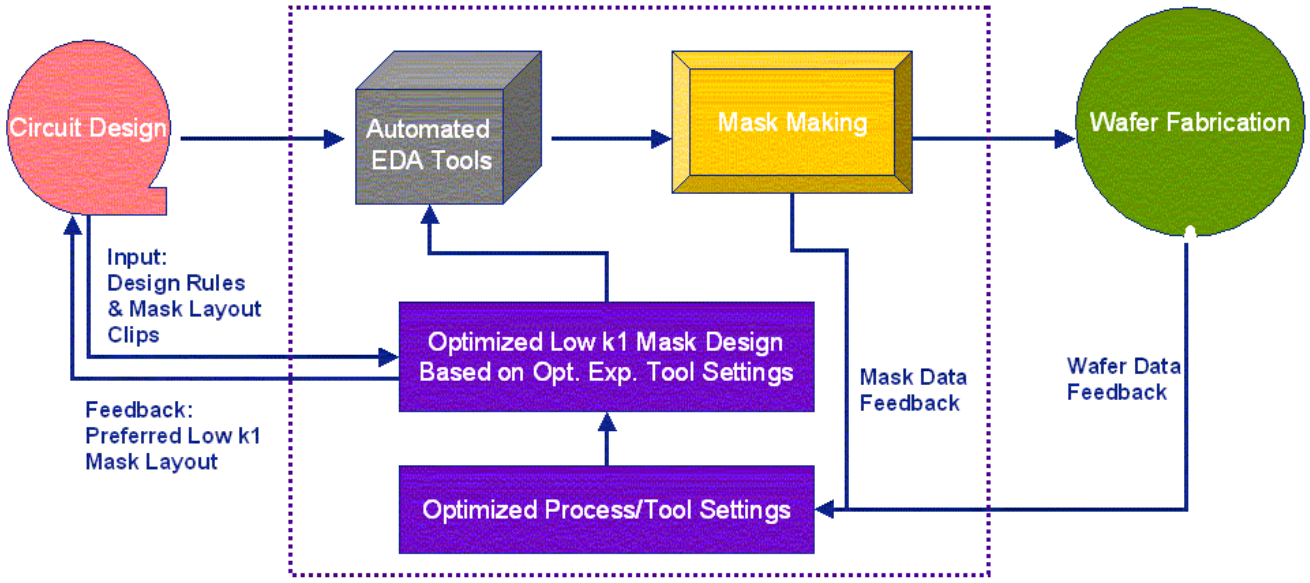

Figure 18: Low k_1 design-to-silicon optimization – from a lithography tool vendor's perspective

13.0 Conclusions

Low k1 imaging may allow the extension of optical lithography to 45 nm. With little doubt, optical lithography will remain the lowest cost method to produce integrated circuits in volume for years to come. However, low k1 will require numerous and severe restrictions on chip design and layout. To continue the success of Moore's Law, the divide in understanding and communications between chip designers and lithographers must be crossed.

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