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GUEST EDITORIAL

Special Section Guest Editorial: 3D Semiconductor Metrology

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The Special Section on 3D Semiconductor Metrology is a collection of nine papers about recent progress on 3D semiconductor metrology, including instrument-based and computational metrology methods. The authors are from some of the major players in the semiconductor industry, including ASML, Bruker, IBM, Intel, KLA, and Lam Research as well as the National Institute of Standards and Technology, University of Michigan, and Eindhoven University of Technology. These papers provide an overview of the state-of-the-art 3D semiconductor metrology for 3D devices currently in high-volume manufacturing and offer a glimpse into the future of metrology for 3D gate-all-around (GAA) transistor and 3D dynamic random-access memory (3D DRAM).

The past decade witnessed the introduction of 3D FinFET and 3D NAND in high-volume manufacturing to continue the historical pace of progress of semiconductor technology. In the future, more complex 3D devices, such as gate-all-around (GAA) transistors and 3D dynamic random-access memories (3D DRAM) will be needed to continue the scaling of semiconductor technology. In 3D GAA transistors, multilayers of 5 nm to 10 nm thin silicon nanosheets/ribbons are stacked vertically, as compared with horizontal fins in FinFET transistors. Gates are wrapped around these silicon nanosheets to offer optimal electrical characteristics of these scaled devices. Like 3D NAND, 3D DRAM will likely require high aspect ratio (with aspect ratios >100:1) channels (and a lithography pitch of >80 nm if 193 nm immersion lithography is required to contain lithography cost). The wall angles of these high aspect ratio deep channels will need to be more than 89°.

As in the case of 3D FinFETs and 3D NAND, the move to 3D GAA transistors and 3D DRAM will come with more complex device shapes, even smaller feature sizes, new materials, and an increased number of parameters needed to characterize the 3D devices and 3D integration technologies. The progress toward 3D device and integration technologies necessitates innovations in semiconductor metrology to meet the challenges of these new 3D device and integration technologies.

The review paper by Wu et al. covers the historical milestones in the invention and development of an x-ray-based metrology technology, called CDSAXS. It employs short wavelength x-rays to non-destructively measure high aspect-ratio, nano-scale critical features on 300-mm wafers, a feat that had been elusive to traditional optical-based metrology methods. CDSAXS has been developed to quantify line height, width, periodicity, sidewall angle, line edge/width roughness, and high aspect ratio structures. Commercial CDSAXS metrology tools entered the market around 2015, after advances in lab x-ray source brightness.

The papers by Gin et al., Sorkhabi et al., and Freychet et al. all describe the use of x-ray scattering for applications such as flash memory hole etch profile and other high aspect ratio parameters, and CD measurements. These papers highlight the increasing importance and broad applicability of x-ray characterization for both inline and lab-based 3D metrology.

The paper by J. Zhang et al. provides an overview of recent advances of 3D metrologies in semiconductor research and development. It describes how methods such as atom probe tomography, transmission electron microscopy, secondary-ion mass spectrometry, x-ray photoelectron

spectroscopy, and optical metrology used to evaluate structure-function relationships and provide 3D information at the device, array, and wafer levels.

The paper by S. Zhang et al. presents sum frequency generation (SFG) vibrational spectroscopy as a 3D chemical metrology to probe buried solid/solid interfaces *in situ* nondestructively. It summarizes recent results obtained from SFG studies on a variety of solid/solid interfaces and chemical reactions at buried solid/solid interfaces as well as structures of buried solid/solid interfaces in multilayered thick devices in semiconductor products.

Hargrove et al. describe the use of process modeling, virtual wafer fabrication, and virtual metrology for process development and accelerated learning for advanced logic and memory. They show how modeling at different stages of device manufacturing help identify variabilities such as 3D NAND pillar etch alignment (including tilt, twist, and bowing), and advanced FinFET logic pitch-walking.

The paper by Houben et al. describes a method of 3D feature reconstruction of nanoscale semiconductor structures from SEM images using synthetic data and machine learning. This data-driven method estimates the height and width (CD) of fin-like structures from a single SEM image. It expands traditional 2D metrology to full 3D surface reconstruction.

The paper by Schmidt et al. gives an overview of a spectral-based technique called vertical traveling scatterometry (VTS). They describe how VTS can be used to simplify optical modeling and overcome geometrical complexities inherent in complex 3D stacks. The papers by Sorkhabi et al., Houben et al., J. Zhang et al., Freychet et al., and Schmidt et al. also show how multiple techniques are used to either obtain new information or validate other methods.

We hope that this JM^3 Special Section on 3D Semiconductor Metrology will serve as a reference for practitioners in the semiconductor industry in resolving issues in metrology, process, production, and yields of current 3D devices. We also hope that this special section will inspire innovations in metrology to future 3D devices and integration technologies. We thank the authors, reviewers, editors, and SPIE staff for their contributions and tireless effort to help produce this JM^3 special section.